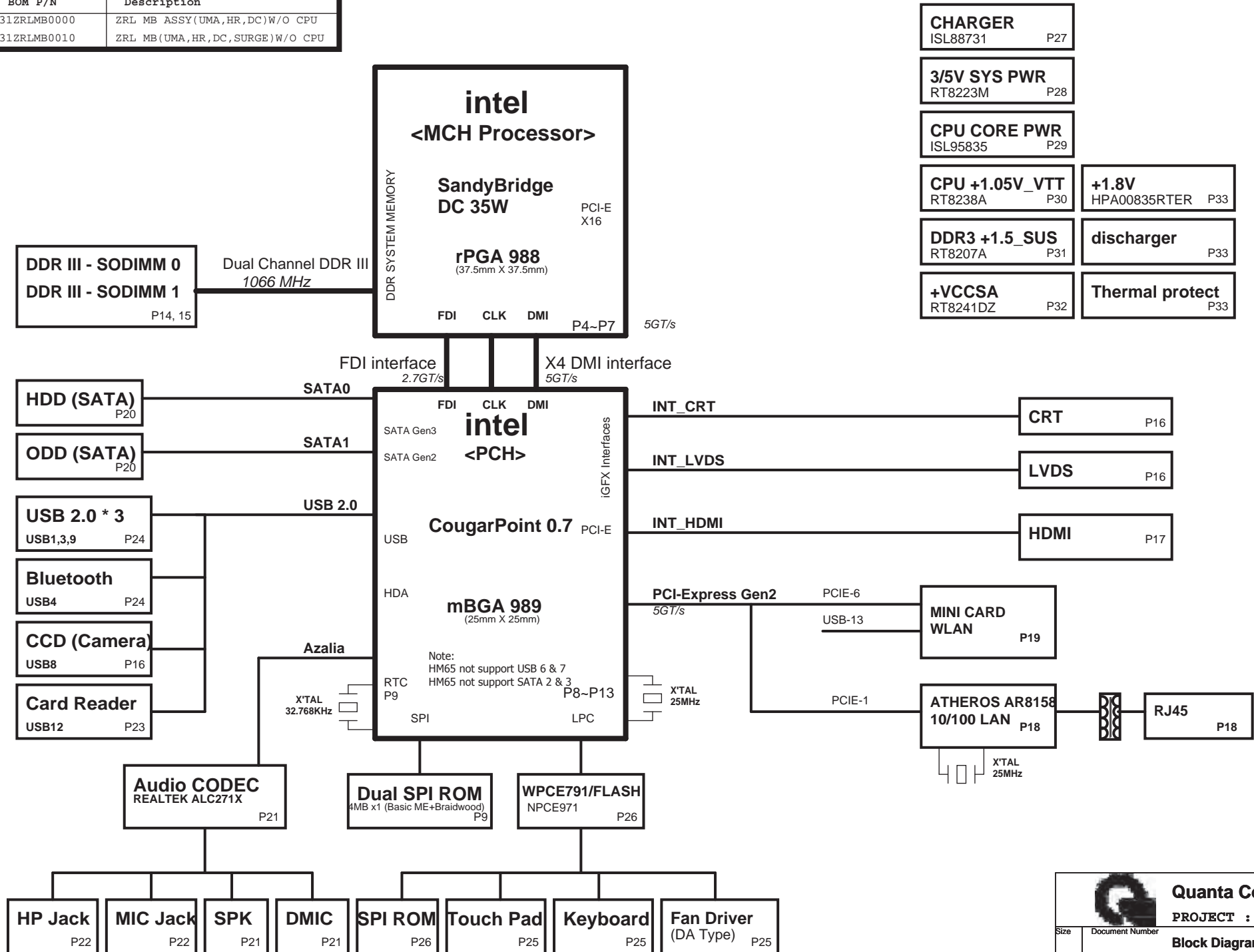


VER : 1A

BOM P/N	Description
31ZRLMB0000	ZRL MB ASSY(UMA,HR,DC)W/O CPU
31ZRLMB0010	ZRL MB (UMA,HR,DC,SURGE)W/O CPU

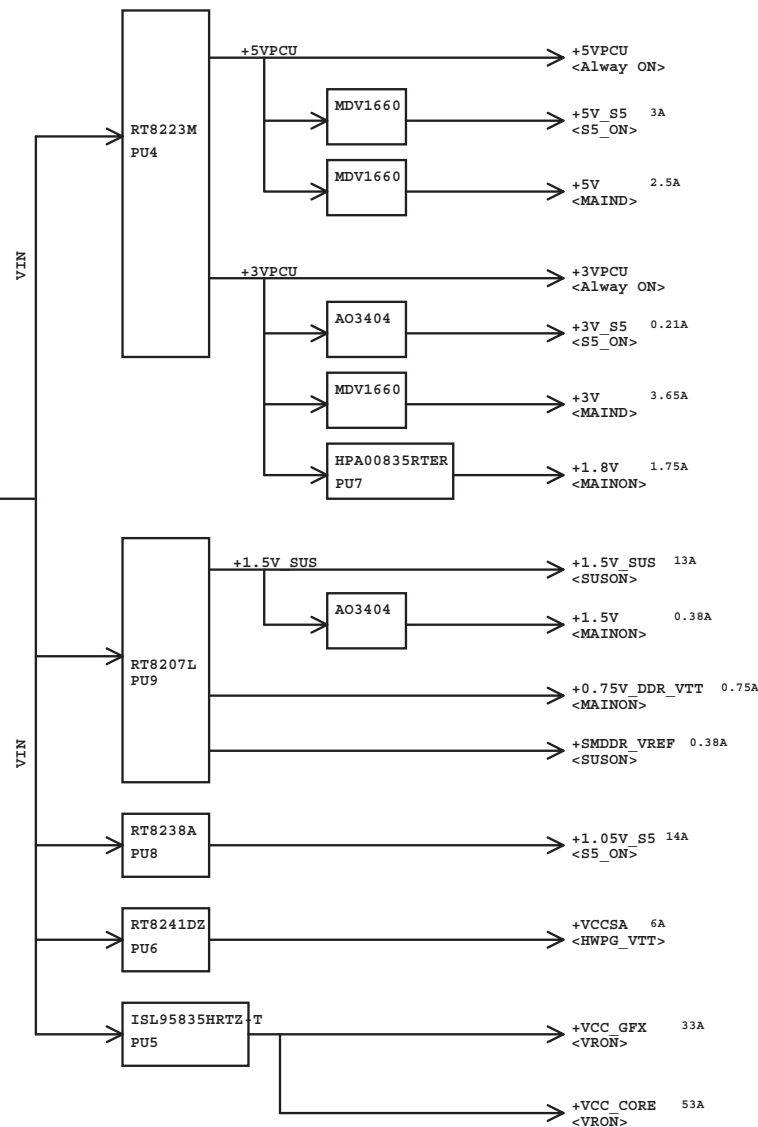
# ZRL BLOCK DIAGRAM



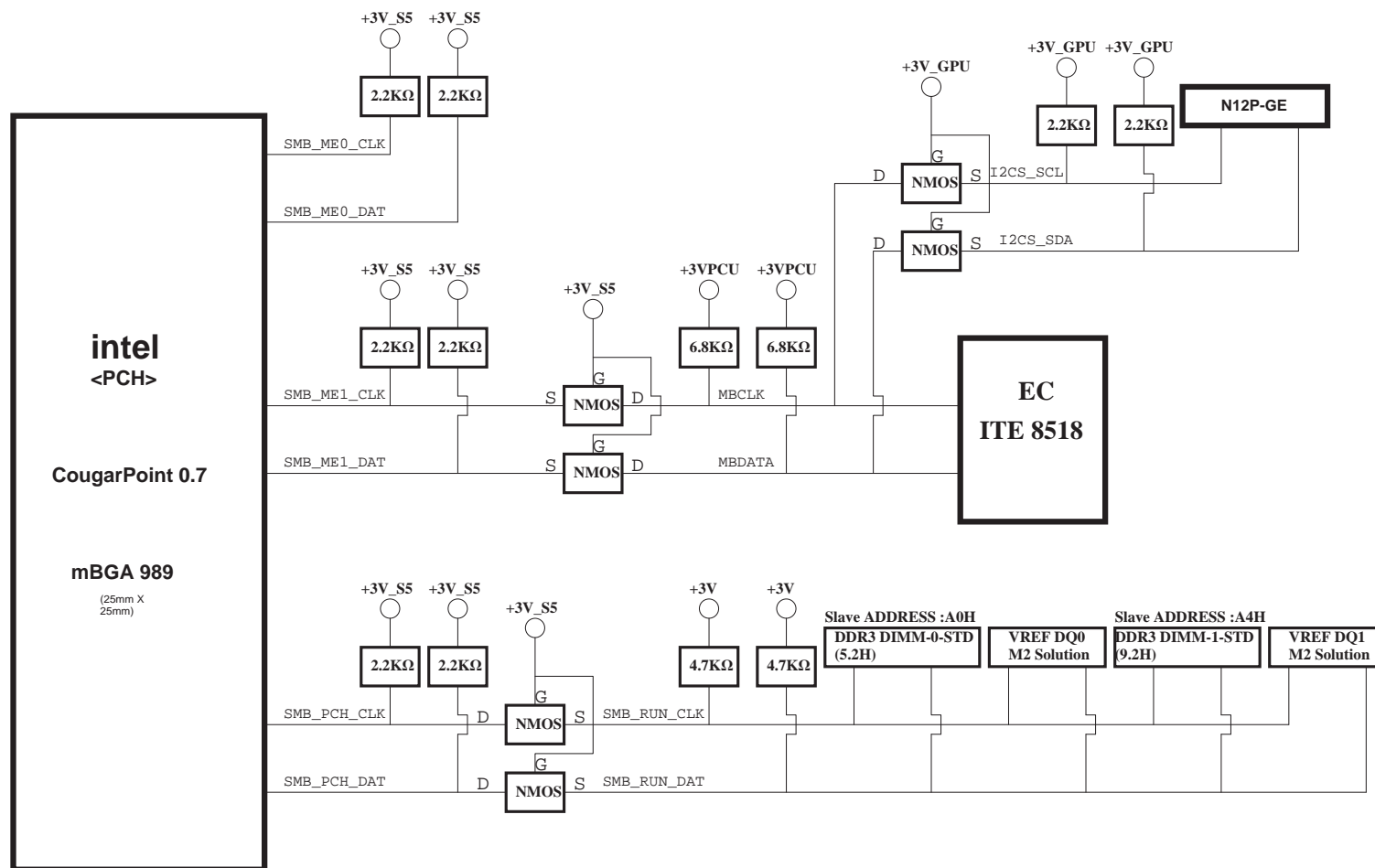
Quanta Computer Inc.

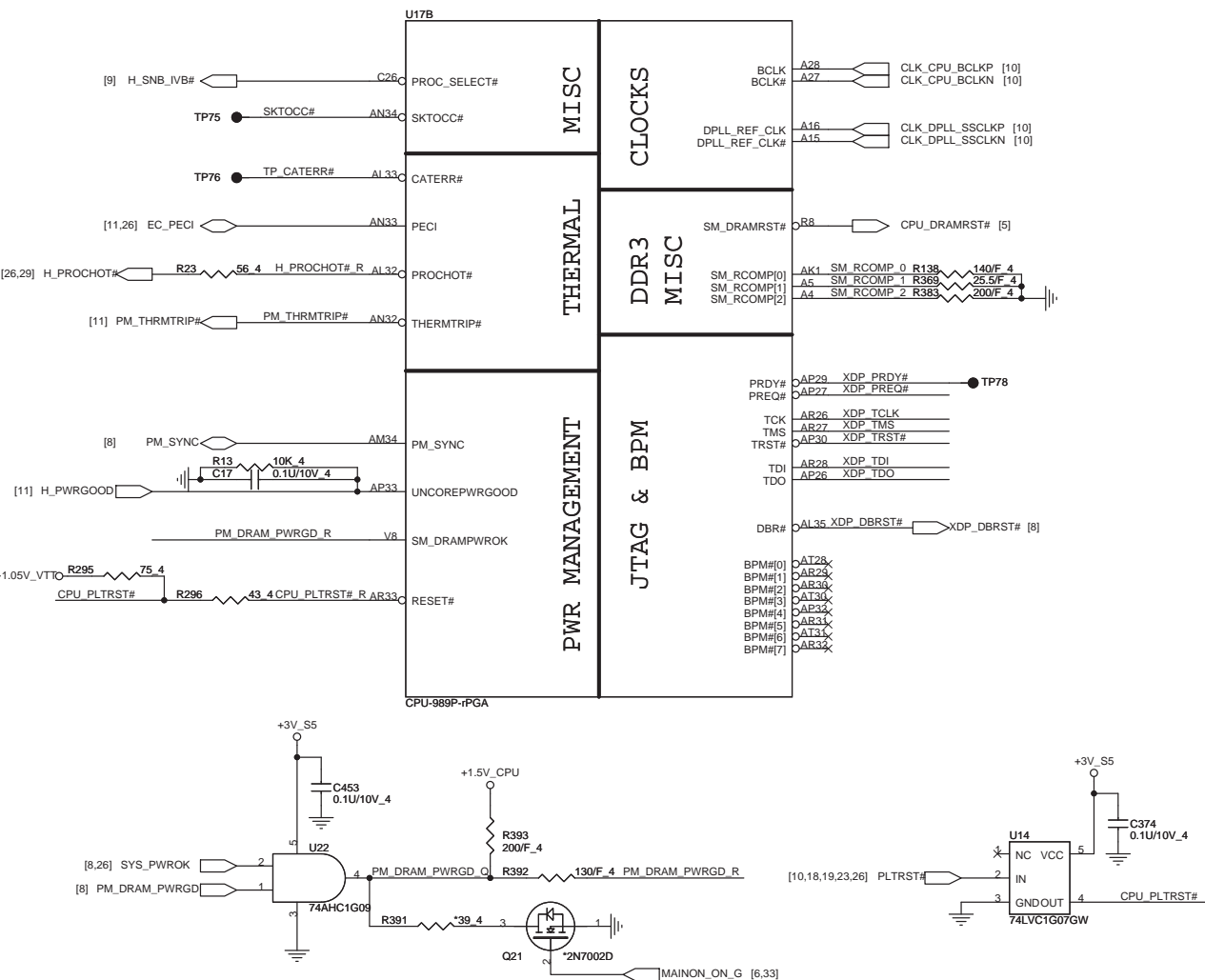
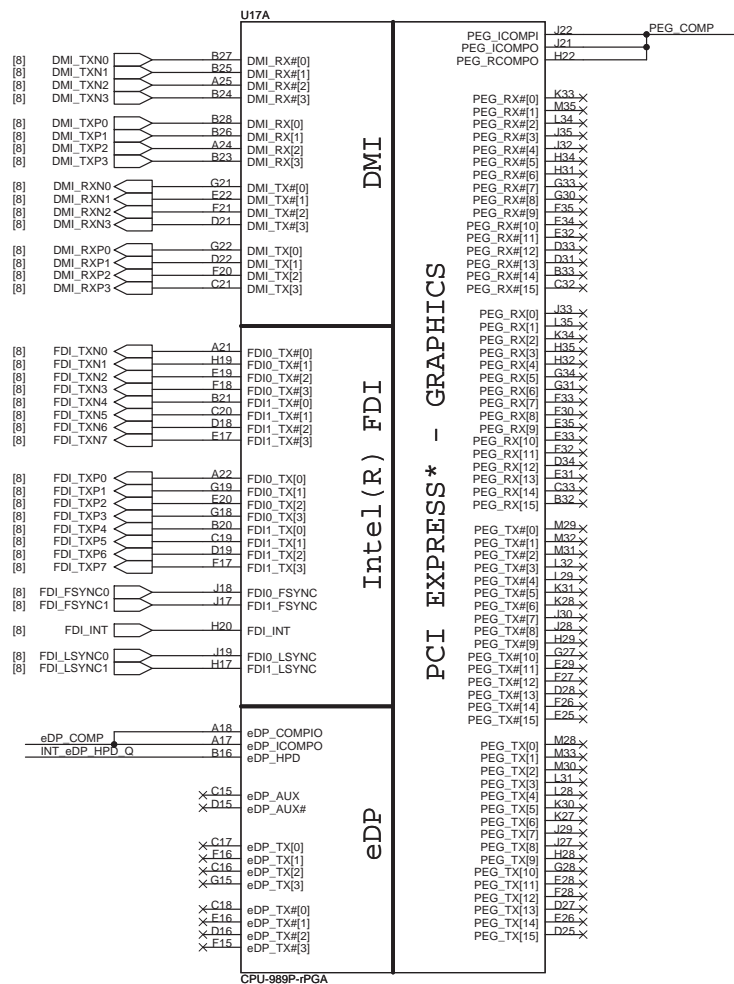
PROJECT : ZRL

WWW.AliSaler.Com

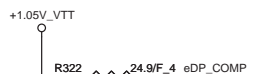


POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V→+19V	MAIN POWER	ALWAYS	ALWAYS
+VCCRTC	+3V~+3.3V	RTC POWER	ALWAYS	ALWAYS
+3VPCU	+3.3V	EC POWER	ALWAYS	ALWAYS
+5VPCU	+5V	CHARGE POWER	ALWAYS	ALWAYS
+15V	+15V	CHARGE PUMP POWER	ALWAYS	ALWAYS
+3V_S5	+3.3V	LANBT/CIR POWER	S5_ON	S0-S5
+5V_S5	+5V	USB POWER	S5_ON	S0-S5
+5V	+5V	HDD/ODD/Codec/TP/CRT/HDMI POWER	MAINON	S0
+3V	+3.3V	PCH/GPU/Peripheral component POWER	MAINON	S0
+1.5VSUS	+1.5V	CPU/SODIMM CORE POWER	SUSON	S0-S3
+0.75V_DDR_VTT	+0.75V	SODIMM Termination POWER	MAINON	S0
+VGFX_AXG	variation	Internal GPU POWER	GPFX_ON	S0
+1.8V	+1.8V	CPU/PCH/Braidwood POWER	MAINON	S0
+1.5V	+1.5V	MINI CARD/NEW CARD POWER	MAINON	S0
+1.1V_VTT	+1.05V or +1.1V	CPU VTT POWER	MAINON	S0
+1.05V	+1.05V	PCH CORE POWER	MAINON	S0
+VCC_CORE	variation	CPU CORE POWER	VIRON	S0
LCDVCC	+3.3V	LCD POWER	LVDS_VDDEN	
+5V_GPU	+5V	SWITCHABLE PVM IC POWER	dGPU_PWR_EN#	Discrete enable
+GPU_CORE	+0.9V~+1.1V	GPU CORE POWER	GPU_F3V_DN	Discrete enable
+GPU_IO	+0.9V~+1.1V	GPU I/O POWER	PG_GPUIO_EN	Discrete enable
+1.5V_GPU	+1.5V	VRAM CORE POWER	PG_1.5V_EN	Discrete enable
+1.8V_GPU	+1.8V	GPU_CRE/LVDS/PLL POWER	+1.5V_GPU	Discrete enable
+1.8V_GPU	+1.8V	DISCRETE GPU POWER	PG_F3V_EN	Discrete enable

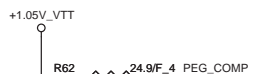




## DP &amp; PEG Compensation



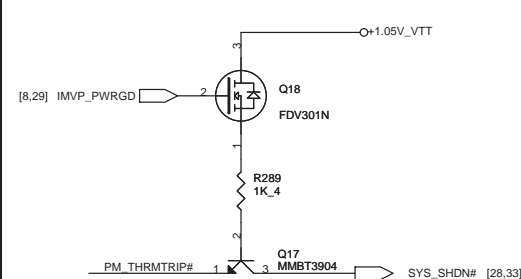
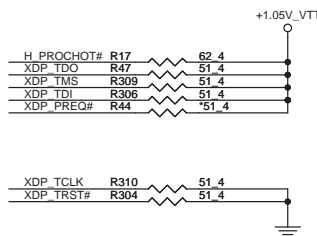
eDP\_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms



PEG\_ICOMPI and RCOMP0 signals should be routed within 500 mils typical impedance = 43 mohms

PEG\_ICOMPO signals should be routed within 500 mils typical impedance = 14.5 mohms

## Processor pull-up(CPU)



## eDP Hot-plug

HPD disable

INT eDP HPD Q



Quanta Computer Inc.

PROJECT : ZRL

Size	Document Number	Rev
	Sandy Bridge 1/4	1A
Date:	Tuesday, June 21, 2011	Sheet 4 of 34

## 05

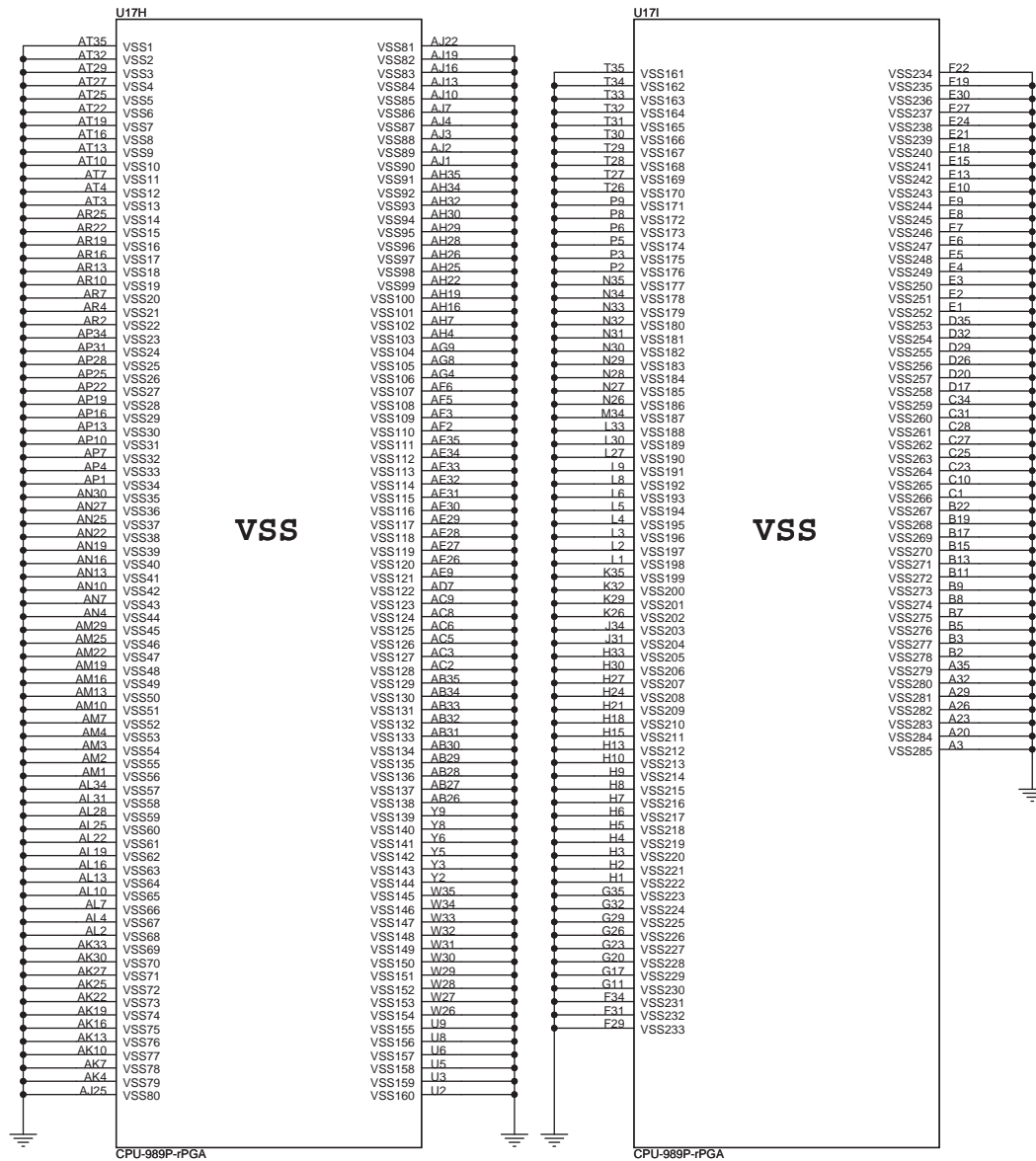


PROJECT : ZRL

Size	Document Number <b>Sandy Bridge 2/4</b>	Rev 1A
Date:	Tuesday, June 21, 2011	Sheet 5 of 34

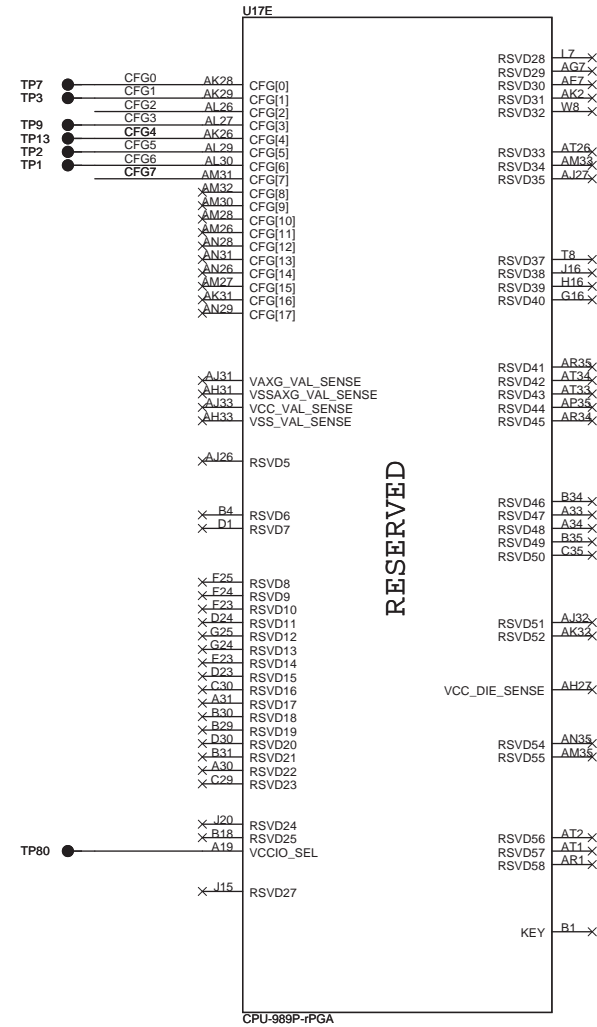


## Sandy Bridge Processor (GND)



## Sandy Bridge Processor (RESERVED, CFG)

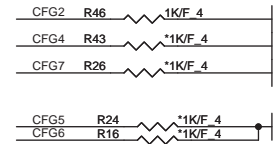
07



## Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training



## CFG[6:5] (PCIe Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled  
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled  
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)  
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



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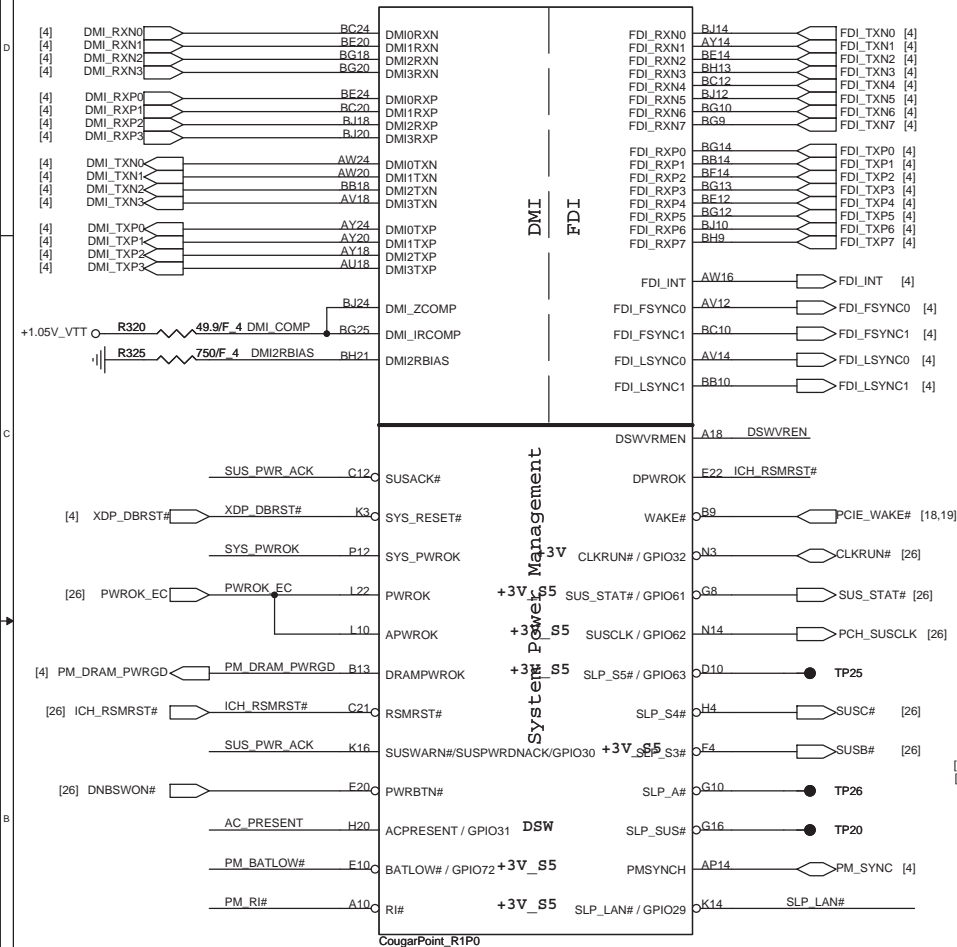
PROJECT : ZRL

Size	Document Number	Rev
	Sandy Bridge 4/4	1A
Date:	Tuesday, June 21, 2011	Sheet 7 of 34



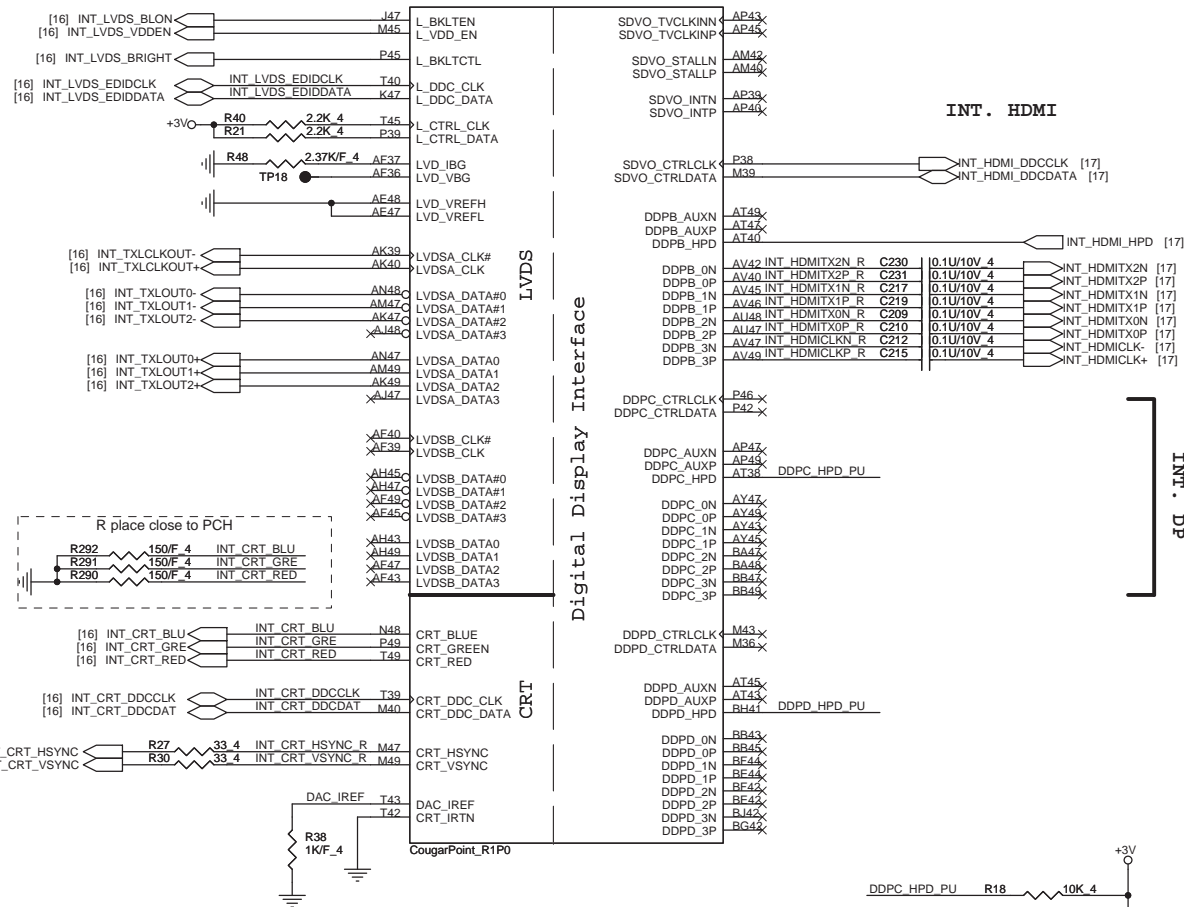
Cougar Point (DMI, FDI, PM)

U16C



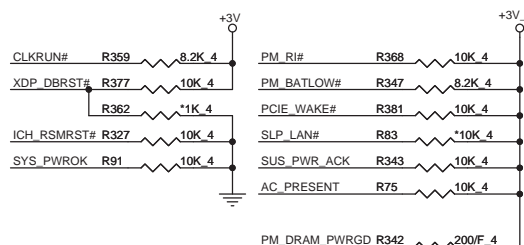
Cougar Point (LVDS, DDI)

U16F

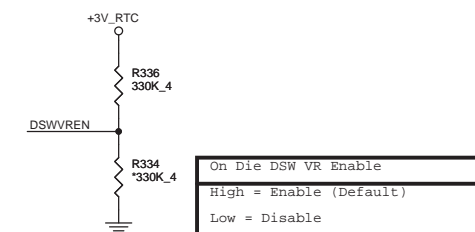
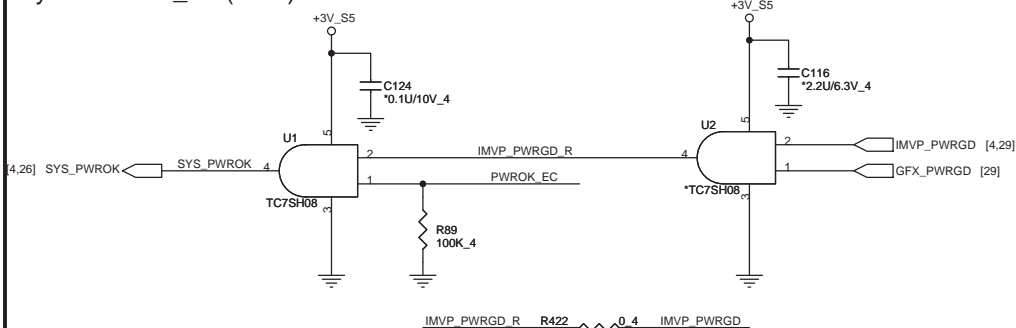


Follow PDG eDP disable guide

PCH Pull-high/low(CLG)



## System PWR\_OK(CLG)

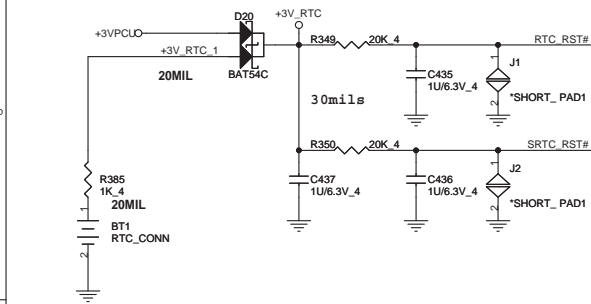


**Quanta Computer Inc.**  
**PROJECT : ZRL**

Size	Document Number	Rev
	<b>Cougar Point 1/6</b>	1
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20mils

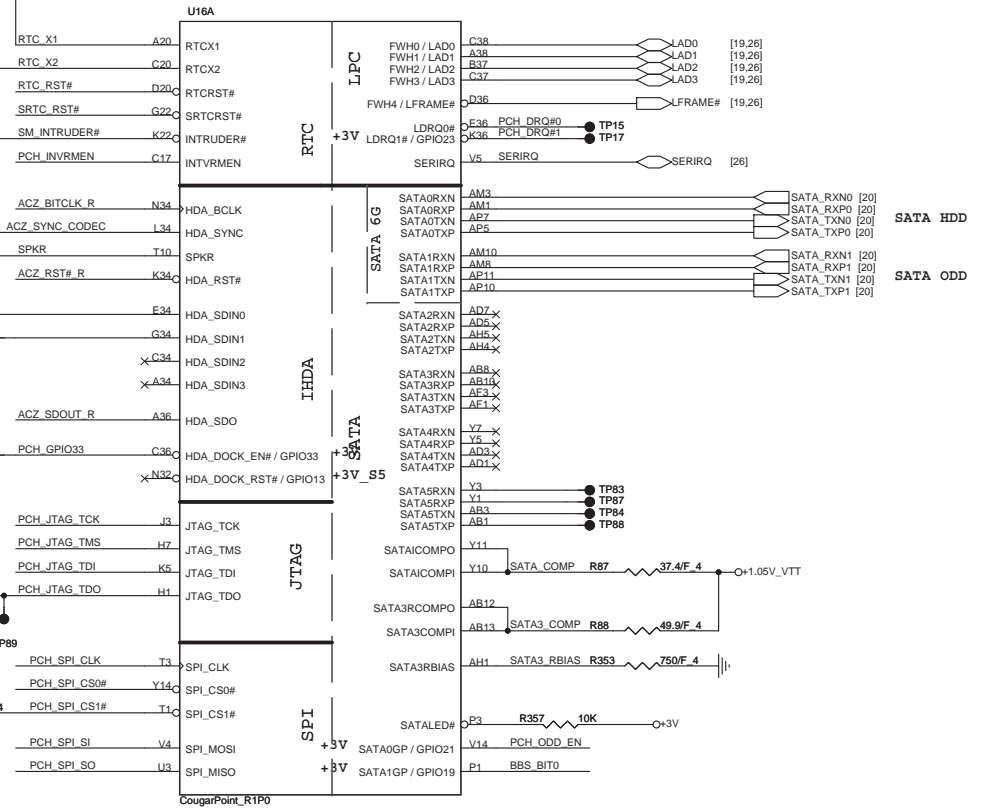


[21]	ACZ_BITCLK	R69	33.4	ACZ_BITCLK R
[21]	ACZ_SYNC	R66	33.4	ACZ_SYNC R
[21]	ACZ_RST#	R65	33.4	ACZ_RST# R
[21]	ACZ_SDOUT	R59	33.4	ACZ_SDOUT R

Schematic diagram of the SPI Flash (U5) circuit. The chip is connected to a 3V3 supply. Pin 1 (CE#) is connected to PCH\_SPI\_CS0#. Pin 2 (SI) is connected to PCH\_SPI\_SI. Pin 3 (WP#) is connected to PCH\_SPI\_SO. Pin 4 (VSS) is connected to ground. Pin 5 (SCK) is connected to PCH\_SPI\_CLK. Pin 6 (SO) is connected to PCH\_SPI\_CS0#. Pin 7 (HOLD#) is connected to pin 4. Pin 8 (VDD) is connected to a 3.3K resistor (R144) to the 3V3 supply. Pin 9 (WP#) is connected to a 3.3K resistor (R145) to the 3V3 supply. Pin 10 (SPI Flash) is connected to ground. A 22pF capacitor (C120) is connected between pins 1 and 2. A 0.1uF capacitor (C143) is connected between pins 8 and 9.

[21] ACZ\_SDIN0 ☐

SERIRQ R108 8.2K 4  
 PCH\_ODD\_EN R105 \*10K 4



Pin Name	Strap description	Sampled	Configuration										
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode										
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)										
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up										
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	<table border="1"> <thead> <tr> <th>GNT1#</th><th>GNT0#</th><th>Boot Location</th></tr> </thead> <tbody> <tr> <td>1</td><td>1</td><td>SPI *</td></tr> <tr> <td>0</td><td>0</td><td>LPC</td></tr> </tbody> </table>	GNT1#	GNT0#	Boot Location	1	1	SPI *	0	0	LPC	
GNT1#	GNT0#	Boot Location											
1	1	SPI *											
0	0	LPC											
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK											
HDA_SDO	Flash Descriptor Security	RSMRST	0 = Override 1 = Default (weak pull-up 20K)										
DF_TVS	DMI/FDI Termination voltage	PWROK	0 = Set to Vss 1 = Set to Vcc (weak pull-down 20K)										
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)										
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V										
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)										
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable										
NV_ALE	Intel Anti-Theft HDD protection	PWROK	0 = Disable (Internal pull-down 20kohm)										

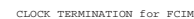
10] **Default weak pull-up on GNT0/1#**  
**[Need external pull-down for LPC BIOS]**



PROJECT : ZRL

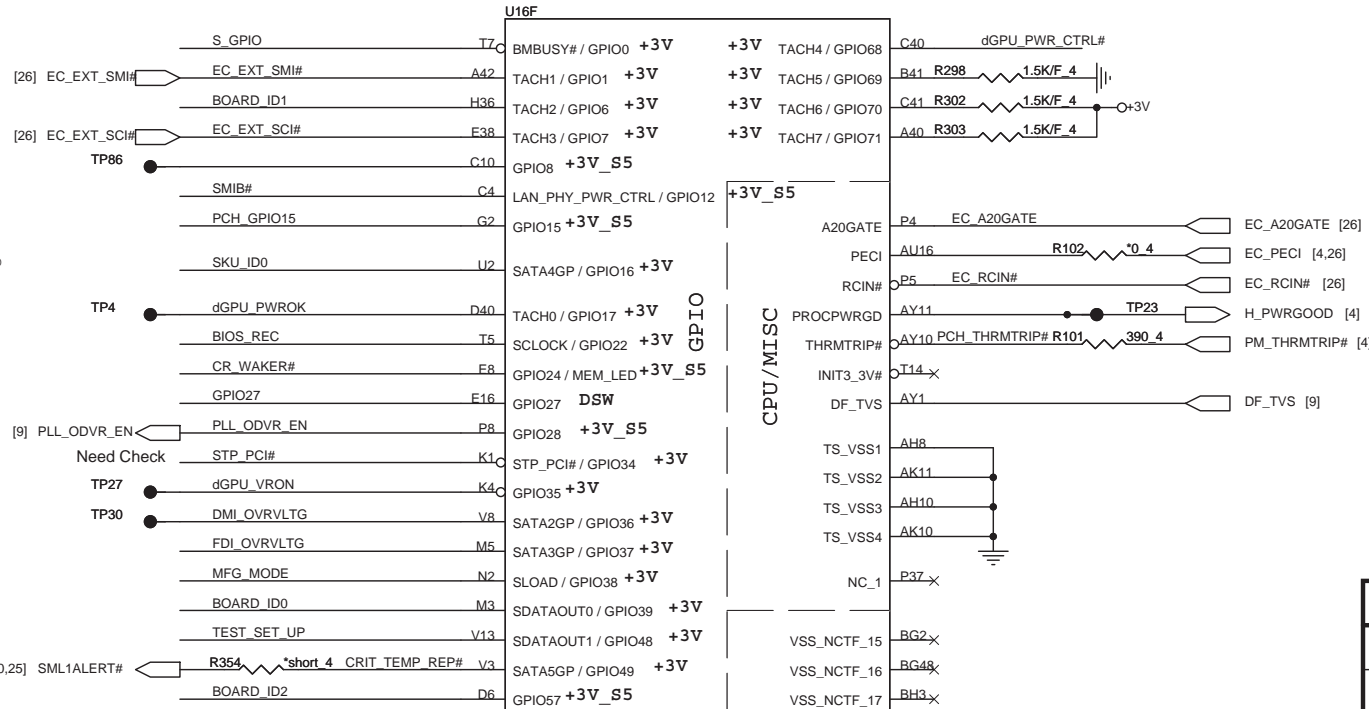
Size	Document Number	Rev
	<b>Cougar Point 2/6</b>	1A
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## U169



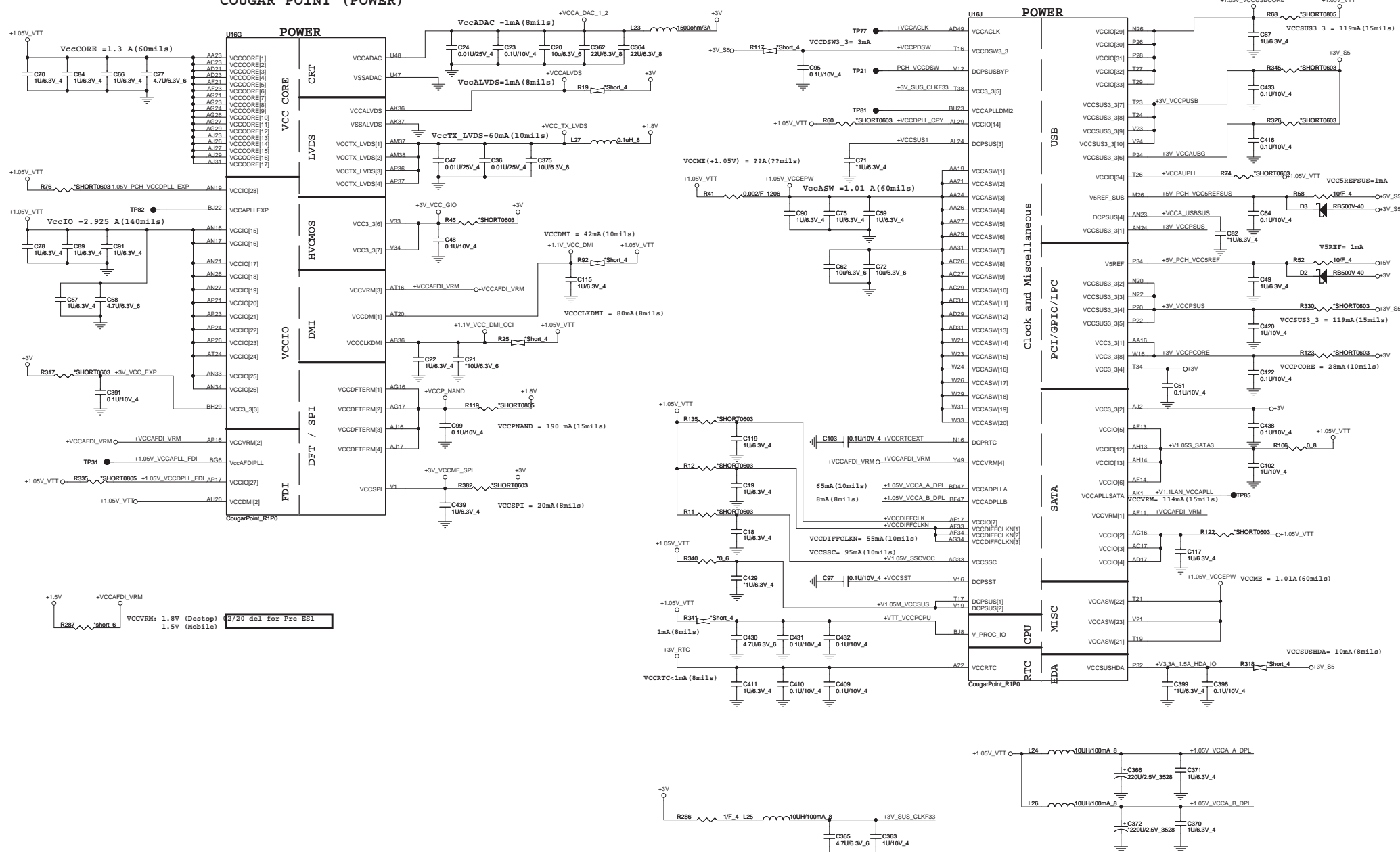
# Cougar Point (GPIO,VSS\_NCTF,RSVD)

11

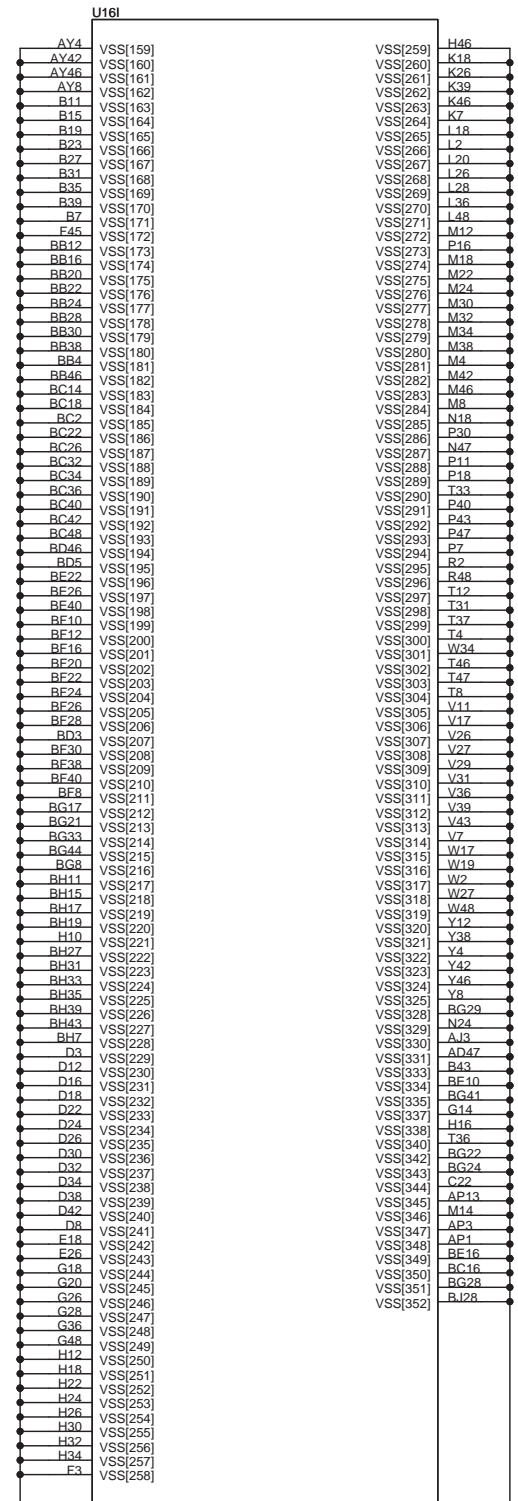
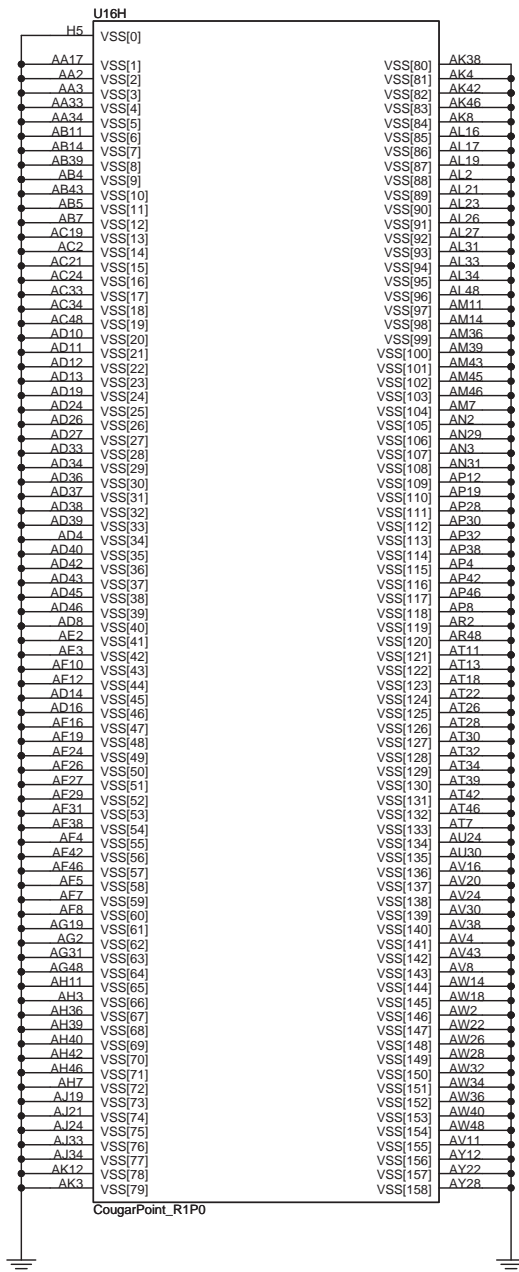


## COUGAR POINT (POWER)

## Cougar Point-M (POWER)

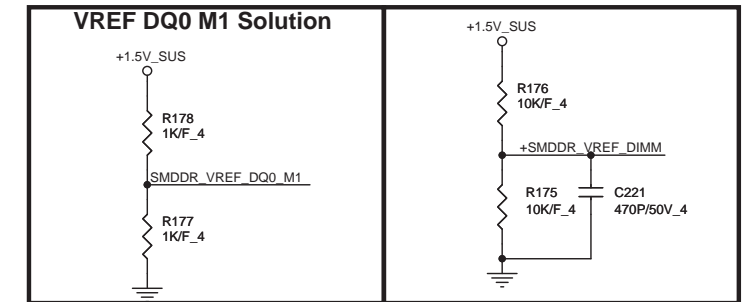
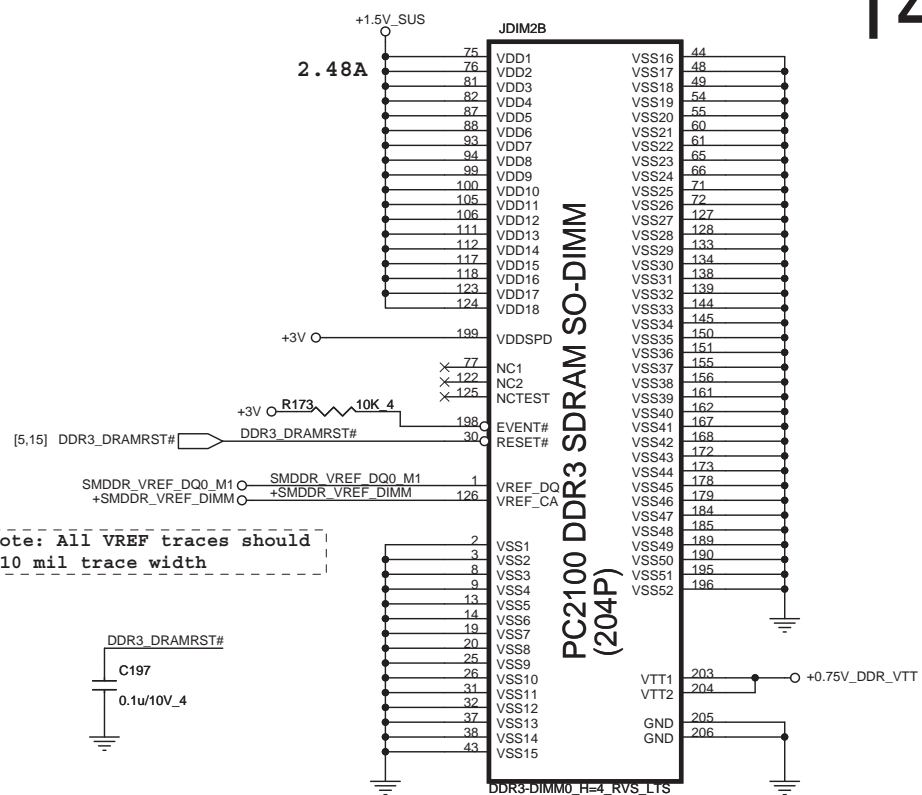
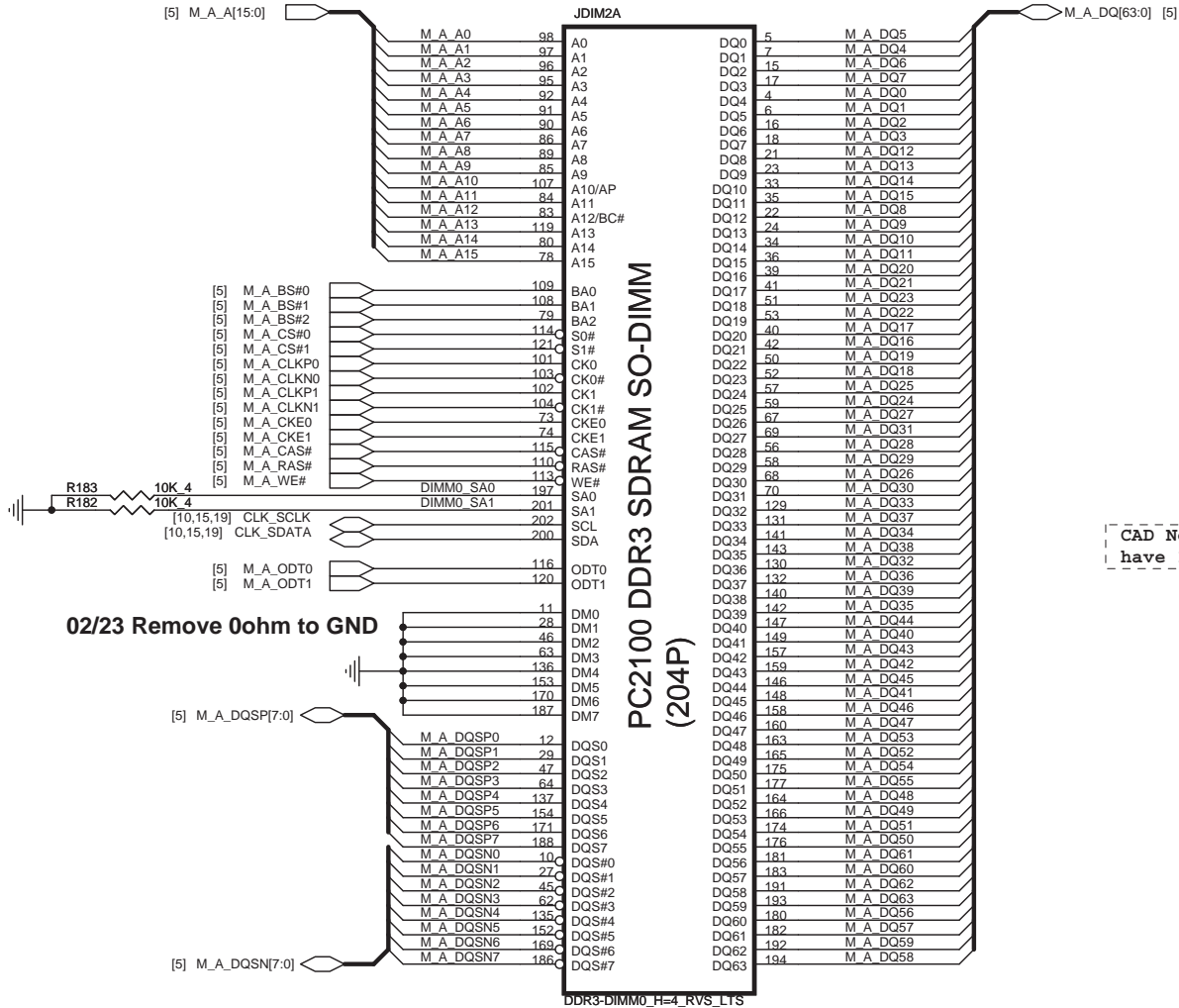


## IBEX PEAK-M (GND)



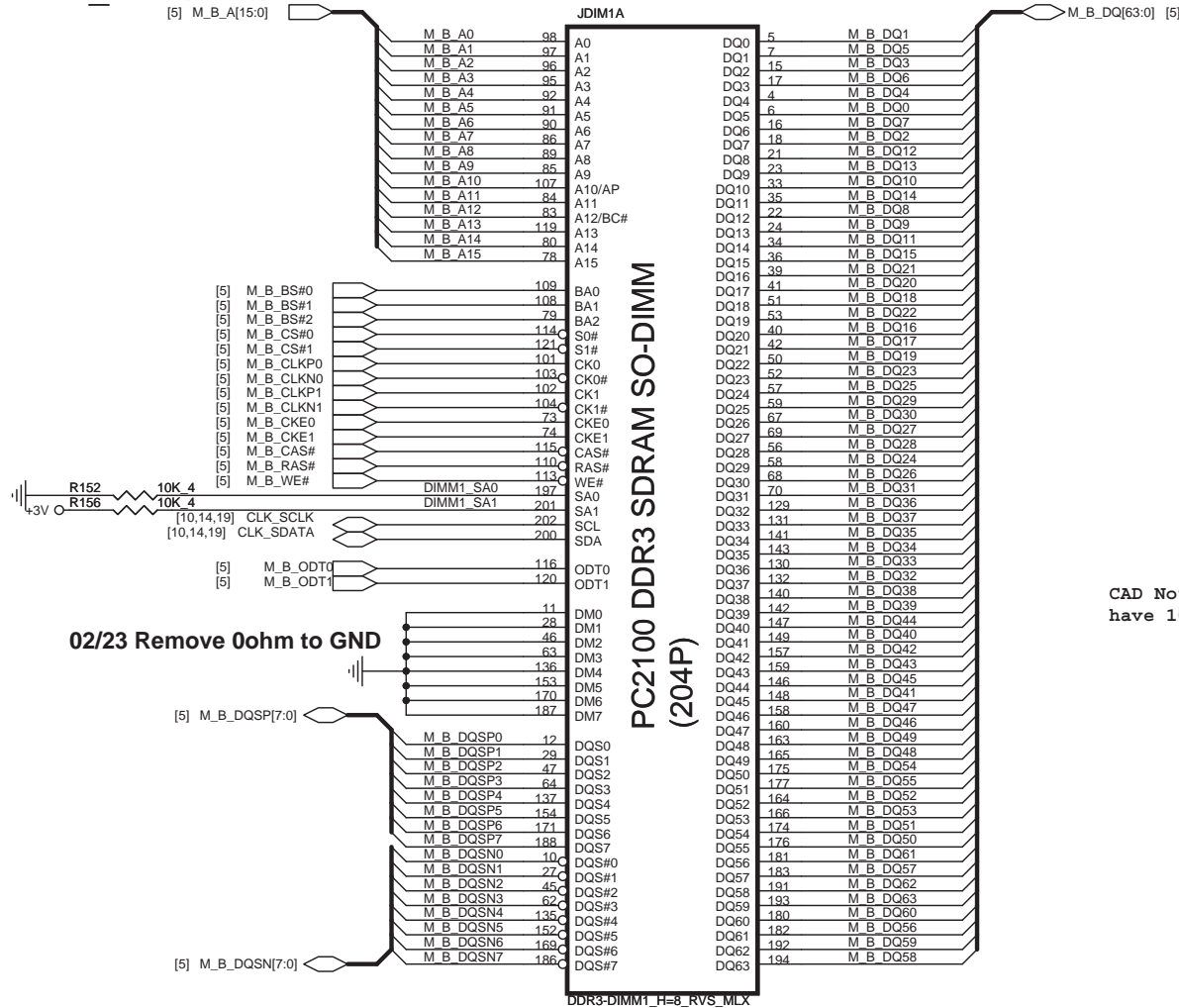


# DDR RVS 4H

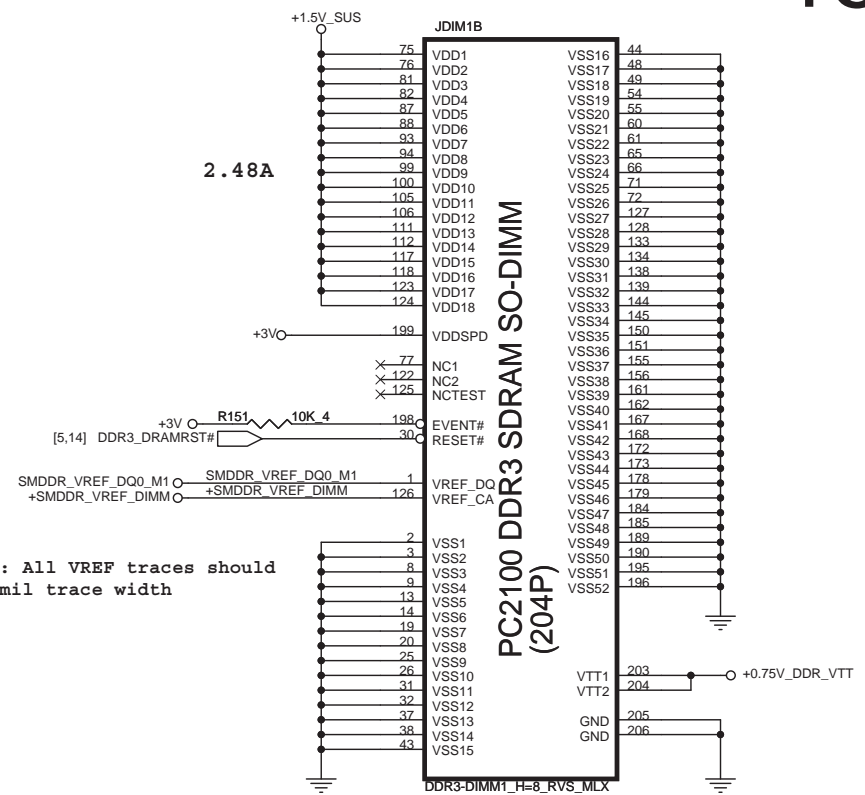




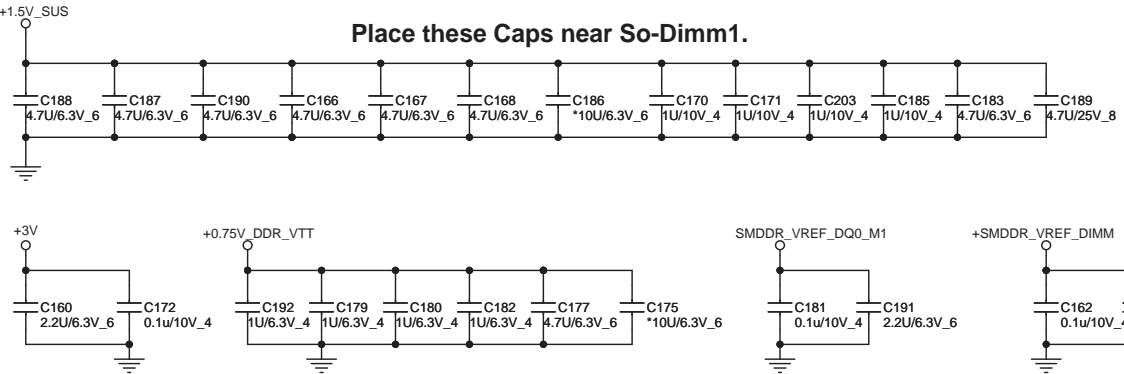
# DDR\_RVS (DDR)



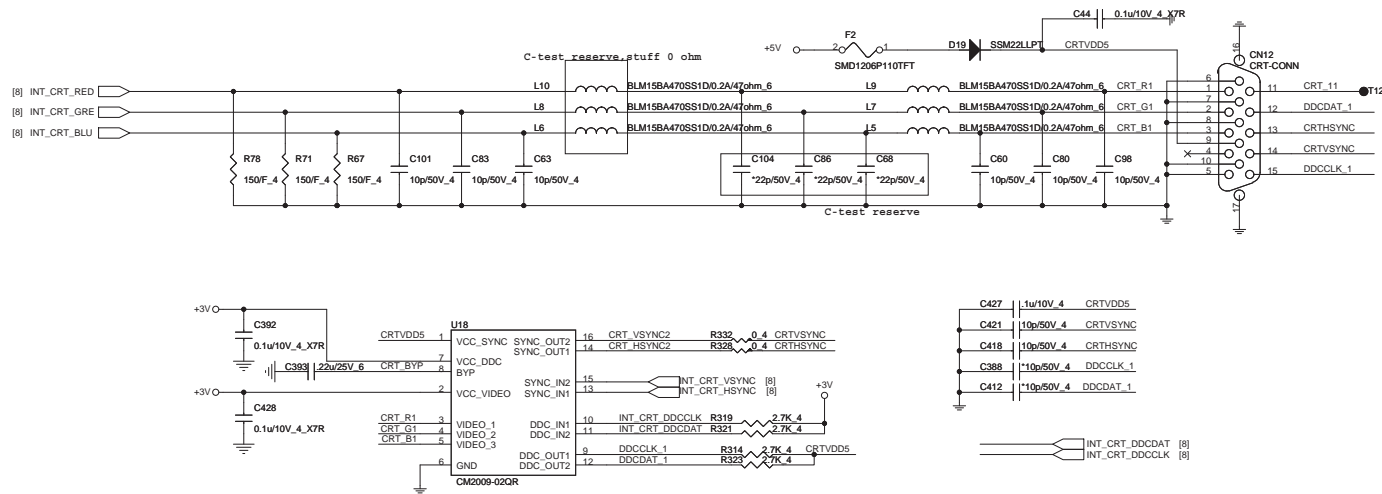
CAD Note: All VREF traces should have 10 mil trace width



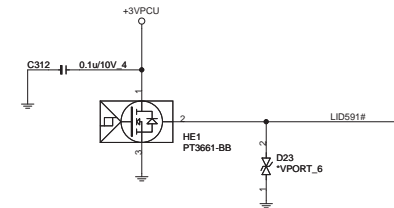
Place these Caps near So-Dimm1.



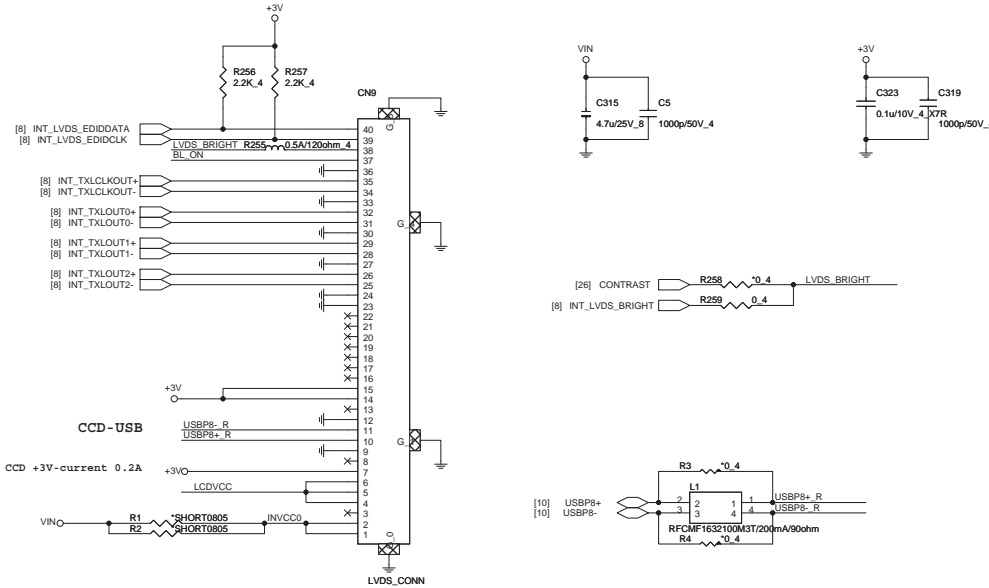
# CRT



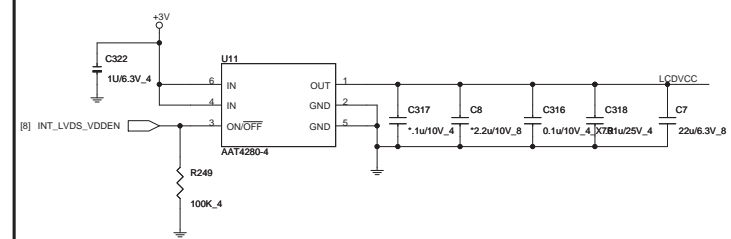
# Lid Switch (Hall sensor)



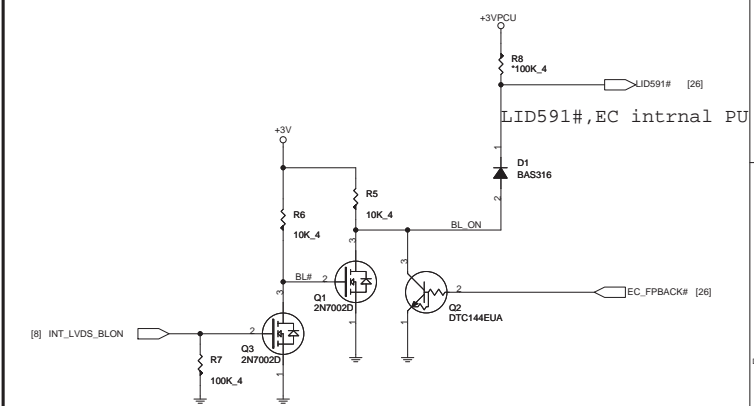
# LVDS



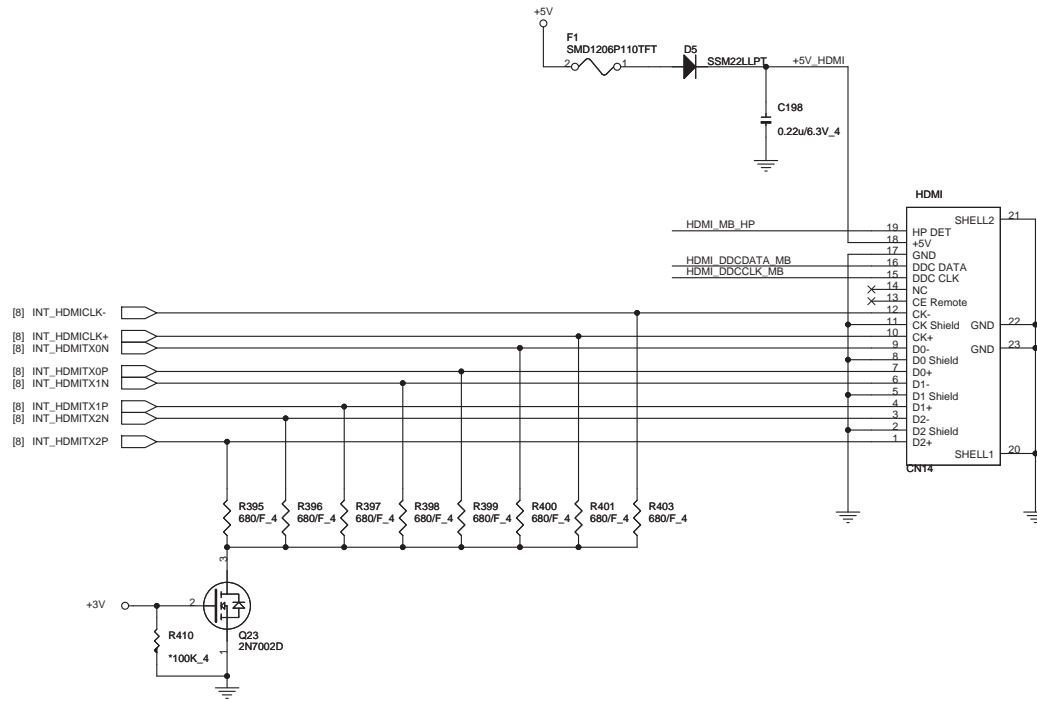
# LCD Power



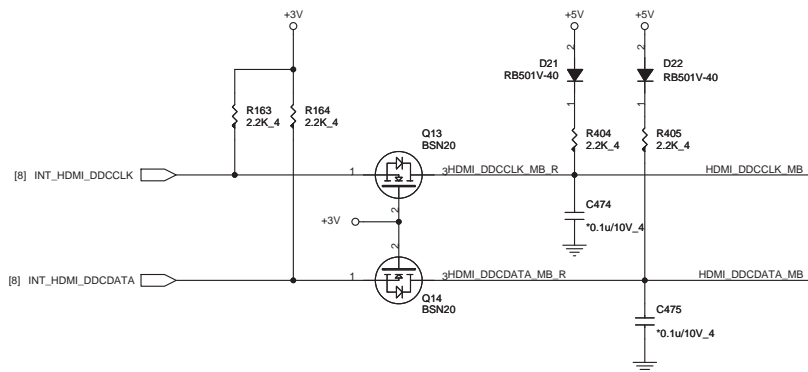
# Backlight Control



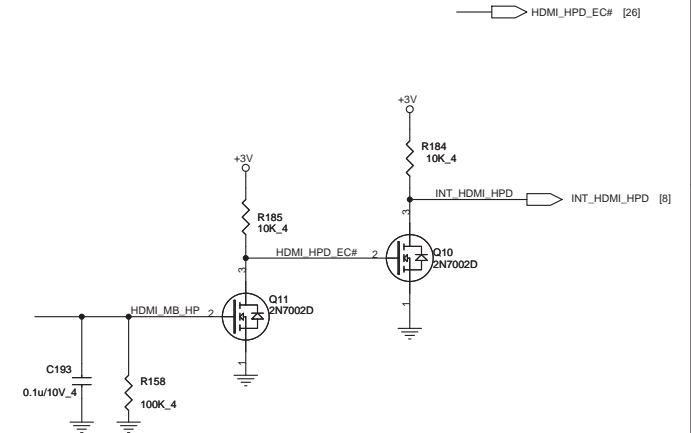
# HDMI



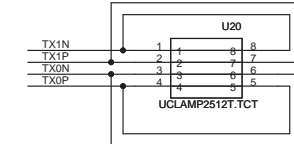
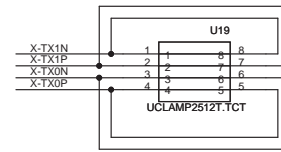
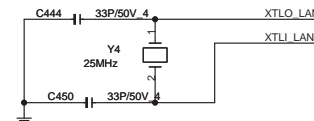
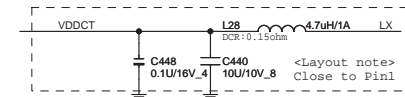
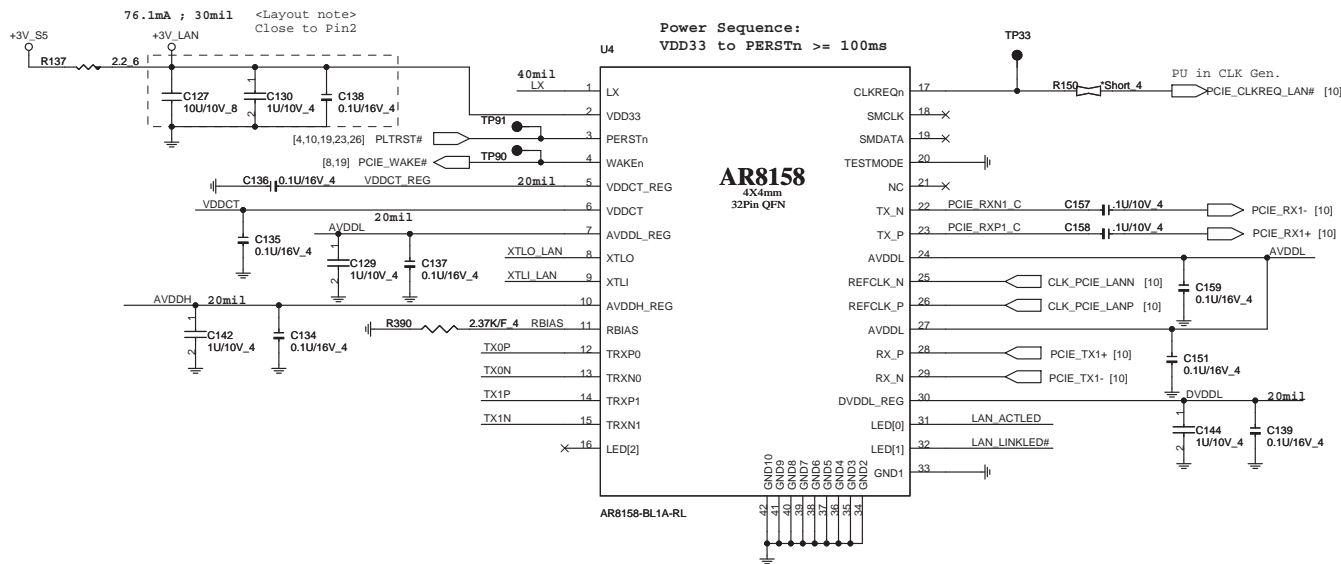
## EMI



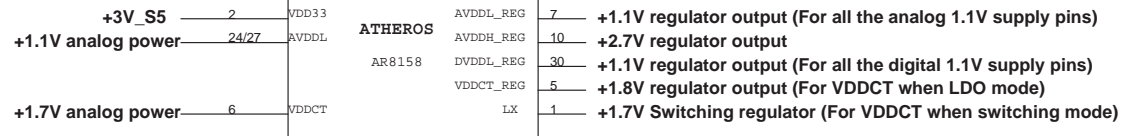
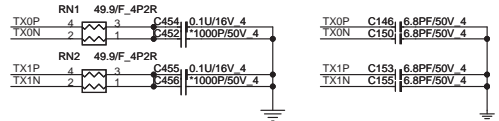
## HDMI-detect



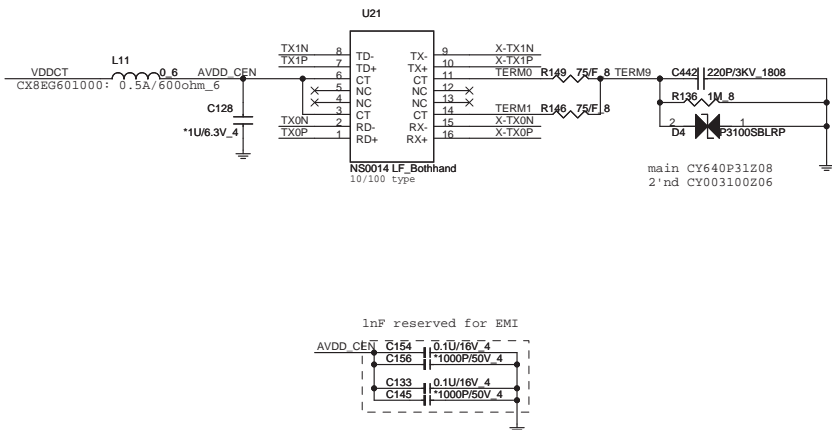
## LAN



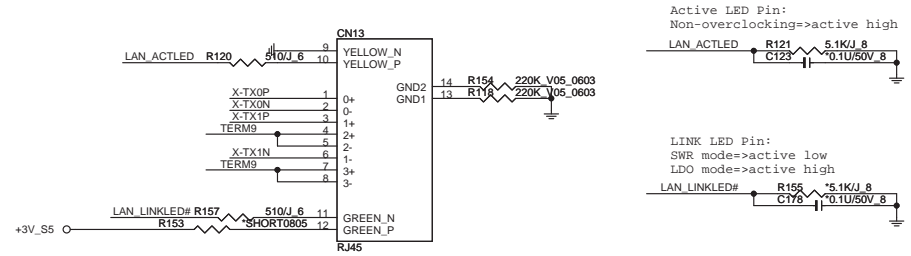
<Layout note>  
Close to LAN Chip 1nF reserved for EMI



# TRANSFORMER



## RJ45 Connector

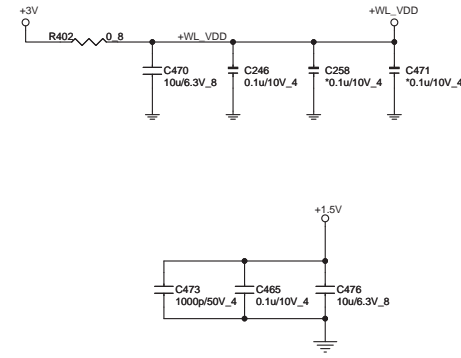
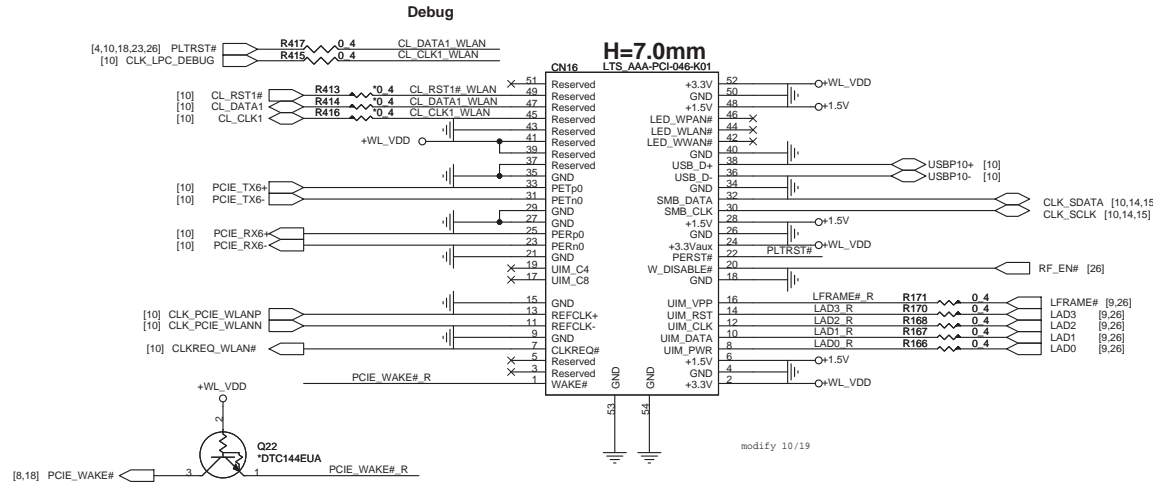
**Quanta Computer Inc.**

PROJECT : ZRL

Size	Document Number <b>LAN AR8158L</b>	Rev 1A
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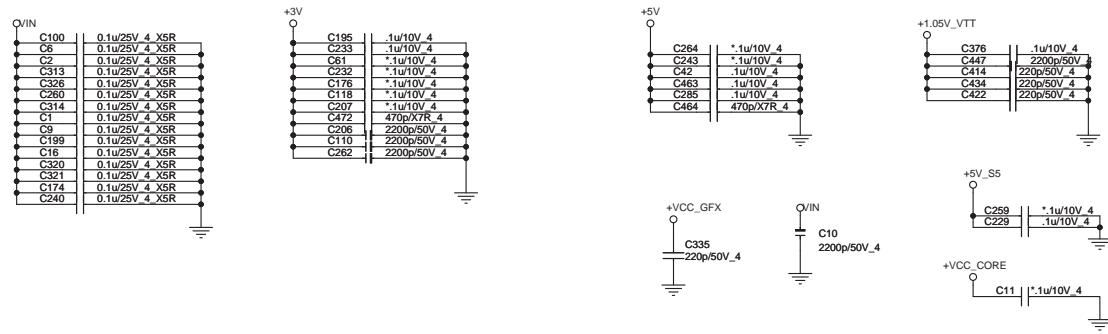
MINI-CARD WLAN

+3.3V: 1000mA  
+3.3Vaux:330mA  
+1.5V:500mA

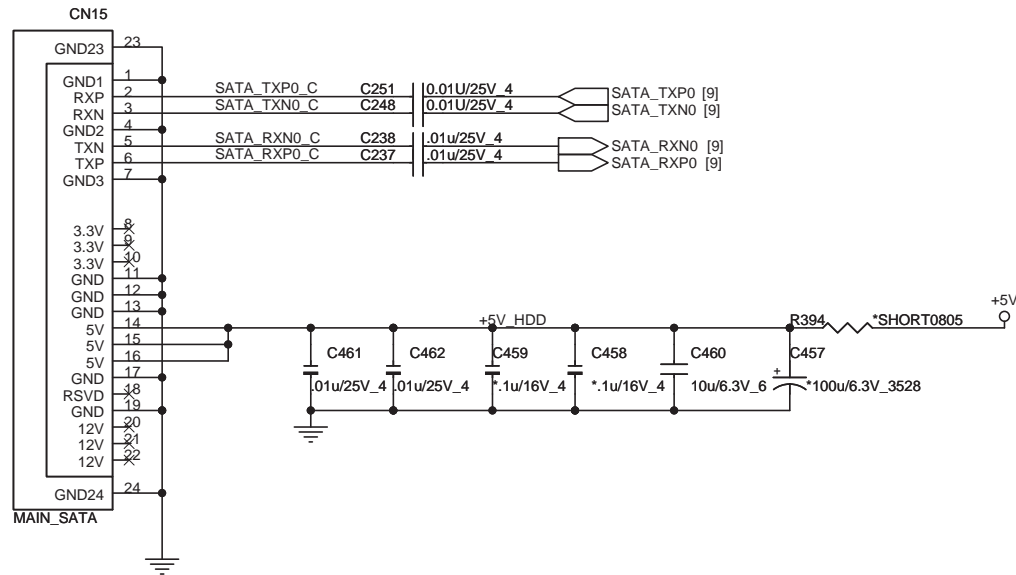


Debug

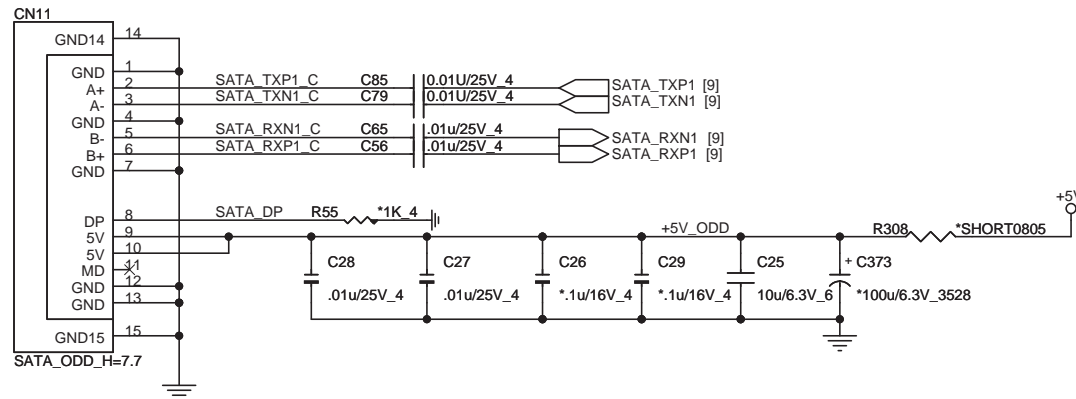
EE RETURN-PATH CAPACITORS




## MAIN SATA HDD



## ODD (SATA)



 <b>Quanta Computer Inc.</b> <b>PROJECT : ZRL</b>		Rev
		1A
Size	Document Number	
<b>SATA-HDD/ODD/USB-ESATA</b>		
Date:	Tuesday, June 21, 2011	Sheet 20 of 34



DIGITAL ANALOG

U23 UPB201200T-310V-N6A/31ohm\_8

IN OUT

GND SHDN SET

C482 \*0.1u/10V\_4

C483 +10u/10V\_3216

C484 \*10u/10V\_3216

C485 \*0.1u/10V\_4

R244 \*0.4

R420 \*29.4K/4

R419 \*10K/4

ADOGND

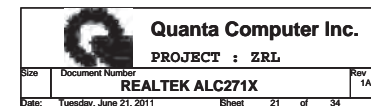
+5V

+5VA

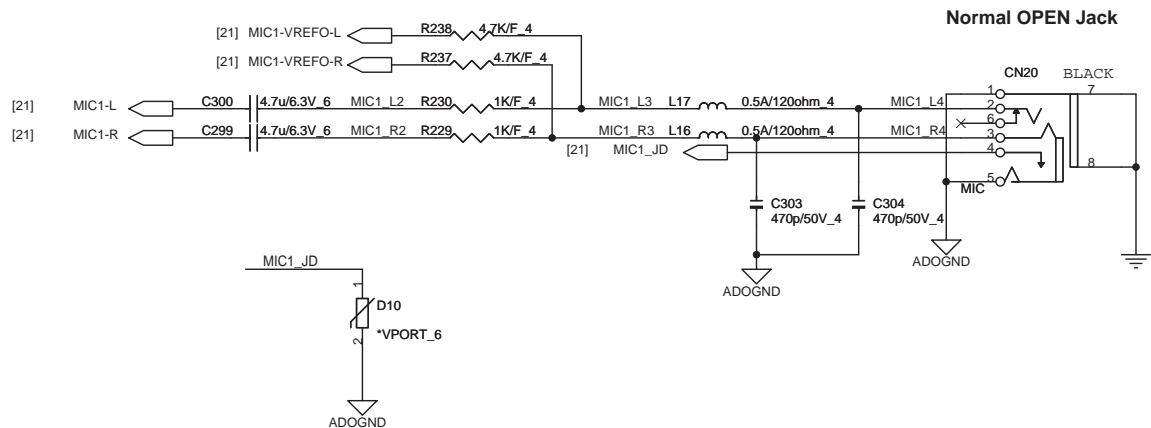
C730, C787 close U37 pin3 and L65

cap place close to MIC-connector

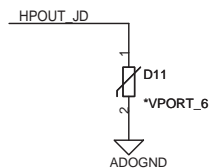
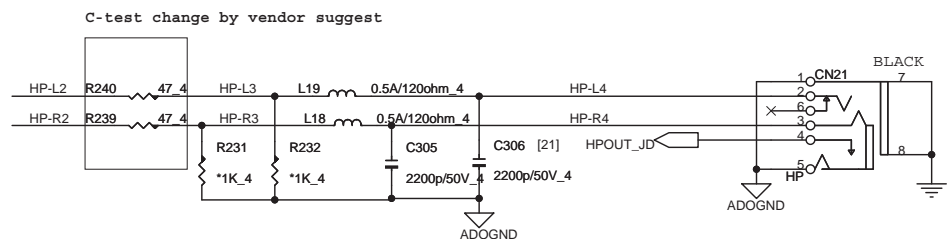
SPEAKER-CONN



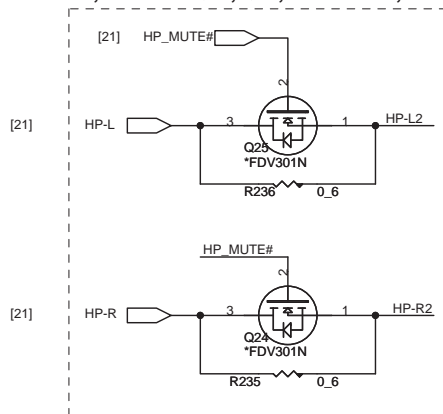
MIC




HP

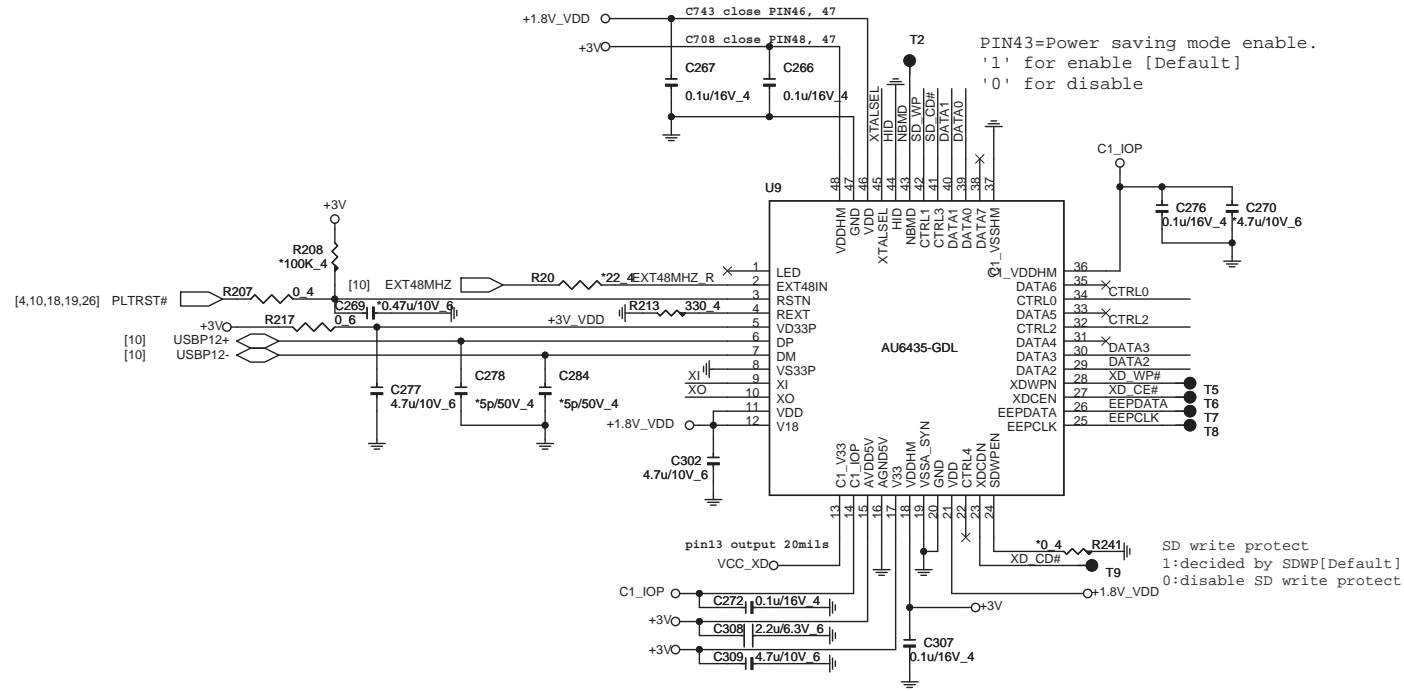


C-test , remove Q25,Q24, stuff R236,R235 fix POPO sound

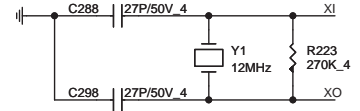


		<b>Quanta Computer Inc.</b>	
		<b>PROJECT : ZRL</b>	
Size	Document Number	<b>AMP /AUDIO JACK CONN</b>	
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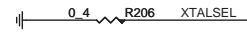
4 in 1 CARD READER IC (SD,MMC,xD,MS)



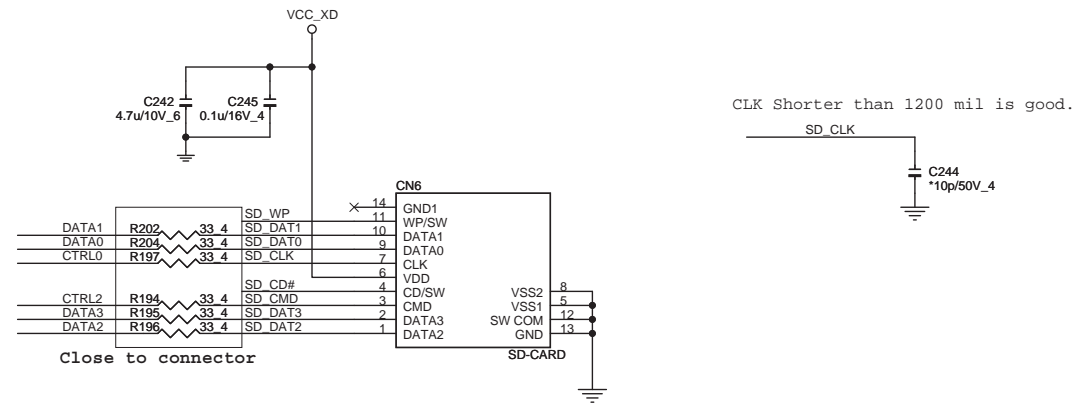
CTRL0, CTRL 1 trace length shorter , and surround with GND.



PIN45=Clock input selection  
'1' for 48MHz input [Default,Internal PU]  
'0' for 12MHz input



2 IN 1 CARD READER CONN (SD/MMC)



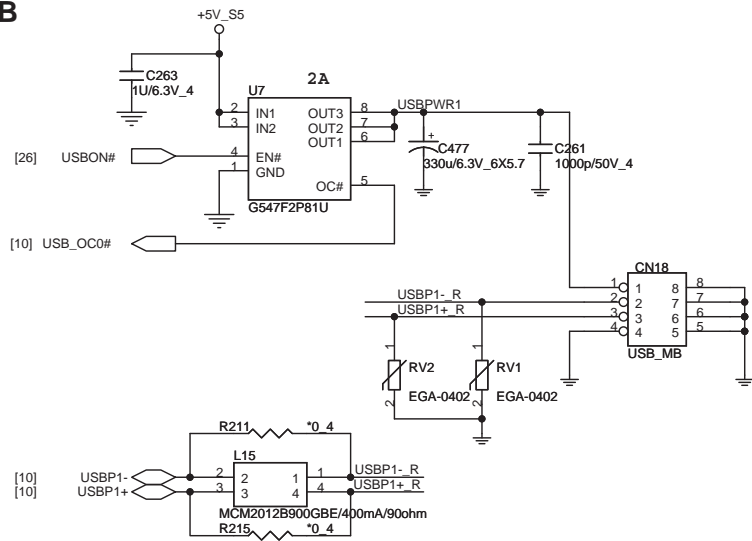
Main	DFHS11FR011
Second	DFHS11FR033



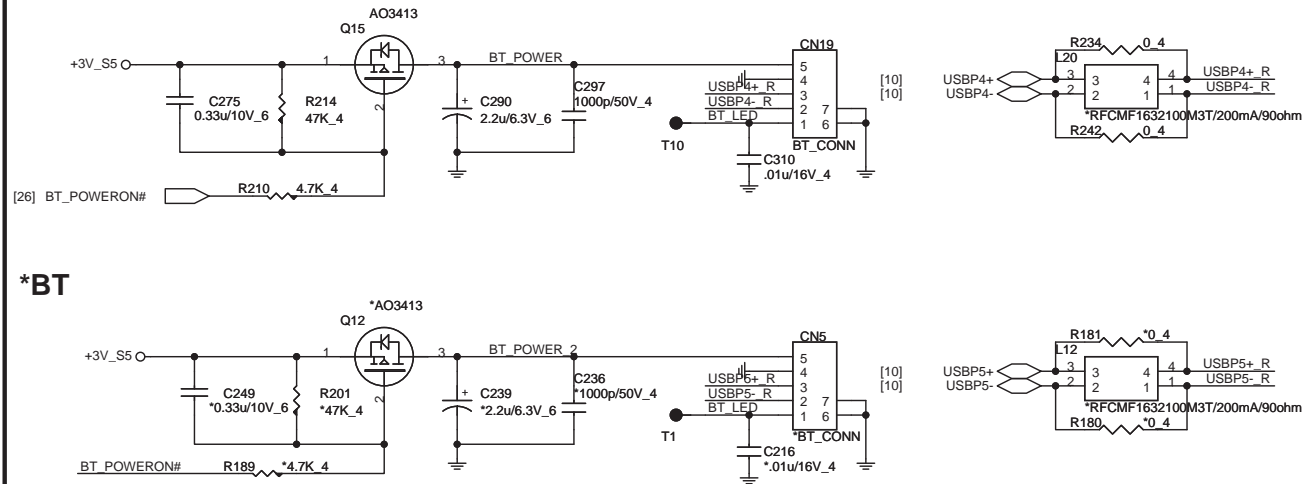
**PROJECT : ZQ5**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>AU6433 CardReader</b>	1A
Date:	Tuesday, June 21, 2011	Sheet 23 of 43

## USB

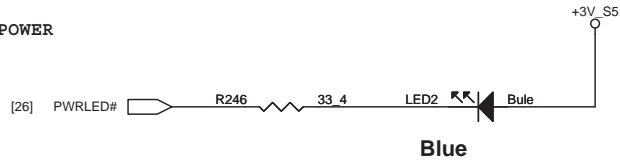


## BT

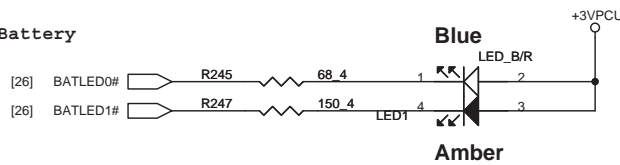


## LED

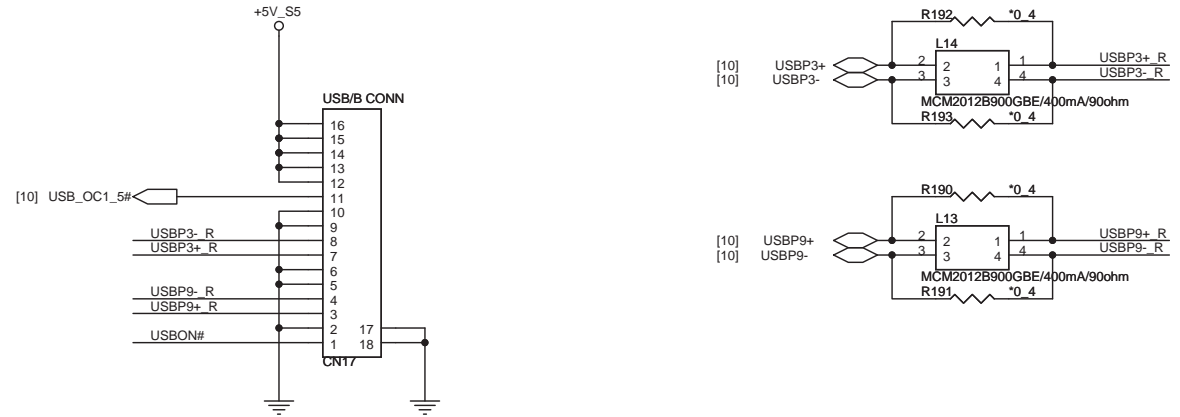
### POWER



### Battery



## USB/B



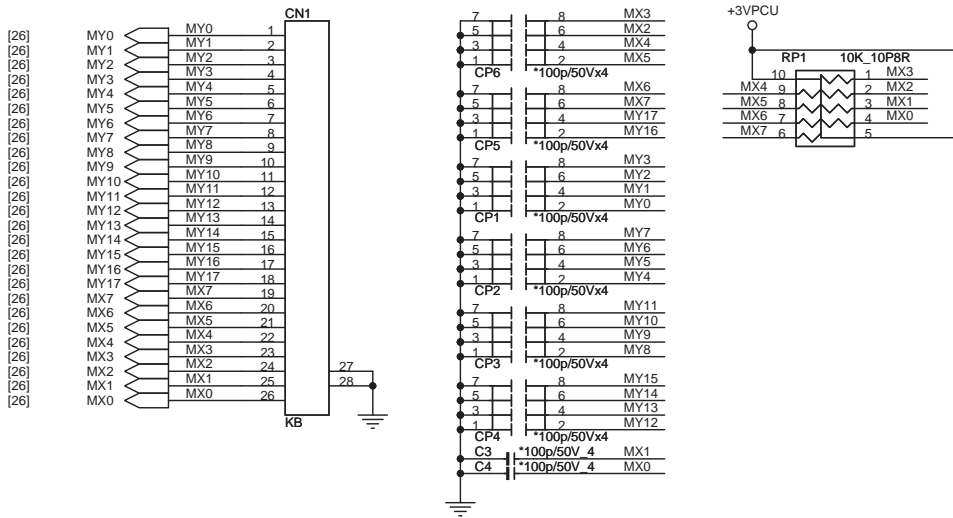
**Quanta Computer Inc.**

**PROJECT : ZRL**

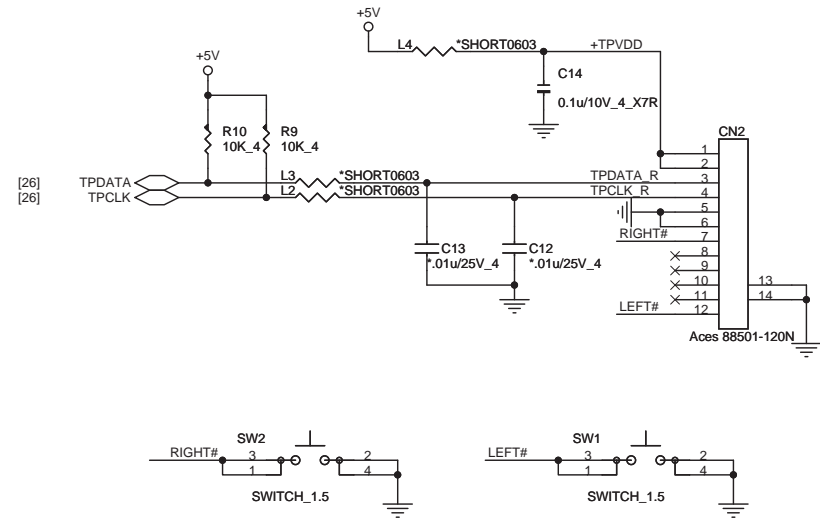
Size	Document Number	Rev
	<b>USB/ BT</b>	1A

Date: Tuesday, June 21, 2011 Sheet 24 of 34

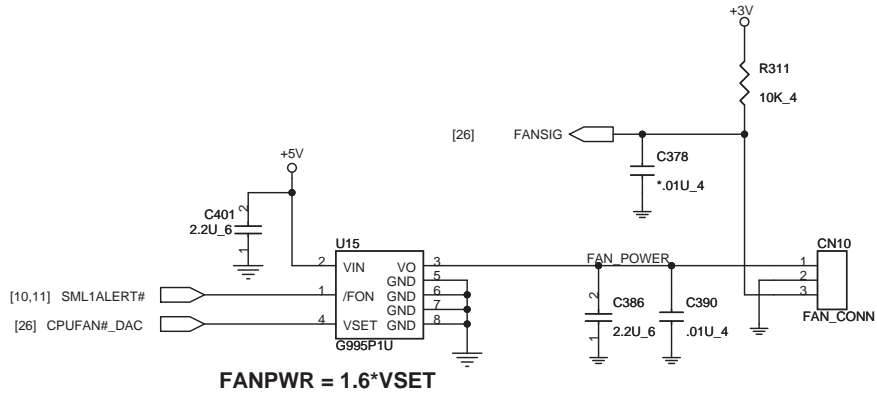
# K/B



# TP

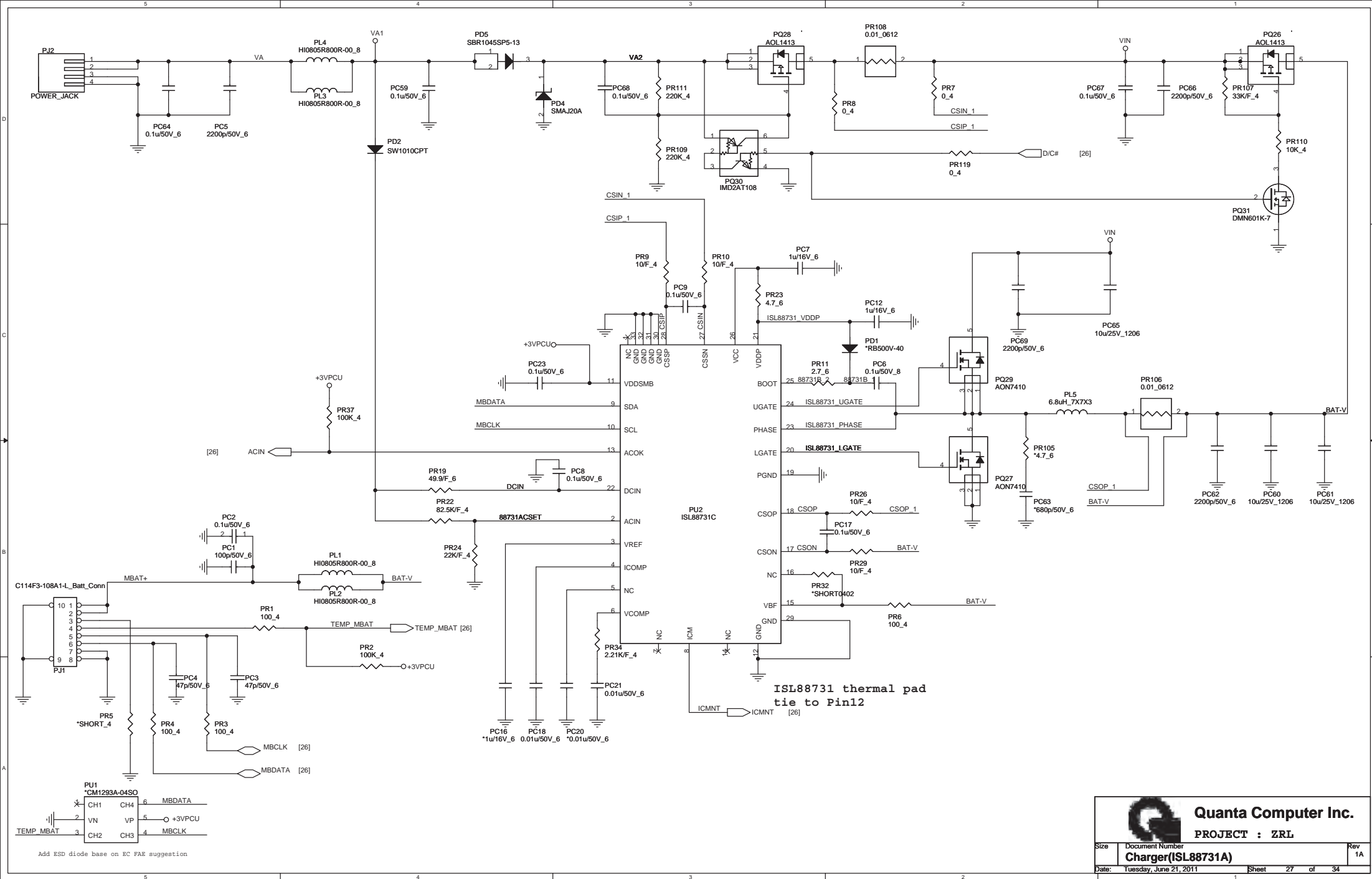


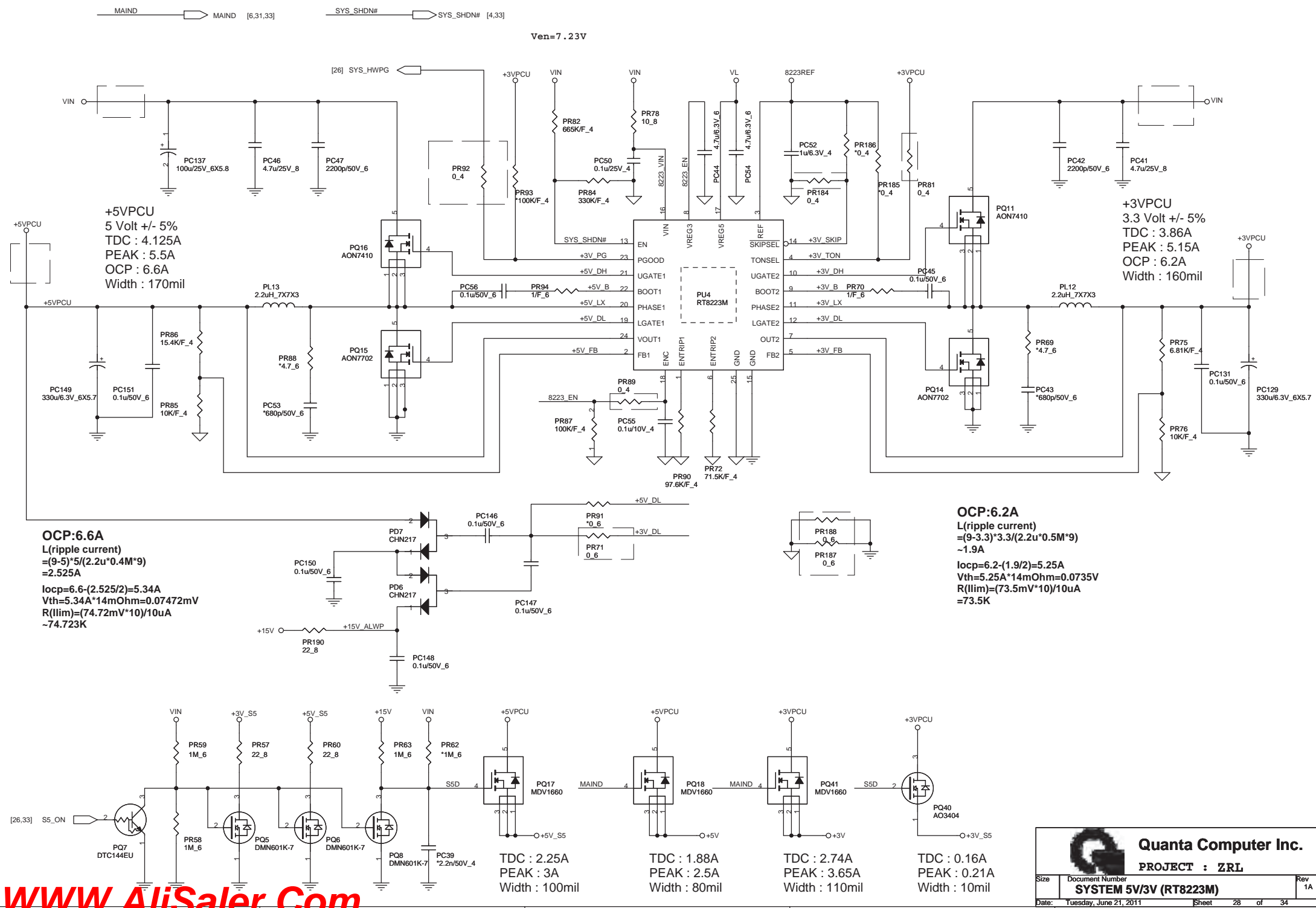
# CPU FAN











**OCP:6.6A**  
L(ripple current)  
=(9-5)\*5/(2.2u\*0.4M\*9)  
=2.525A  
Iocp=6.6-(2.525/2)=5.34A  
Vth=5.34A\*14mOhm=0.07472mV  
R(lim)=(74.72mV\*10)/10uA  
~74.723K

**OCP:6.2A**  
L(ripple current)  
=(9-3.3)\*3.3/(2.2u\*0.5M\*9)  
~1.9A  
Iocp=6.2-(1.9/2)=5.25A  
Vth=5.25A\*14mOhm=0.0735V  
R(lim)=(73.5mV\*10)/10uA  
=73.5K

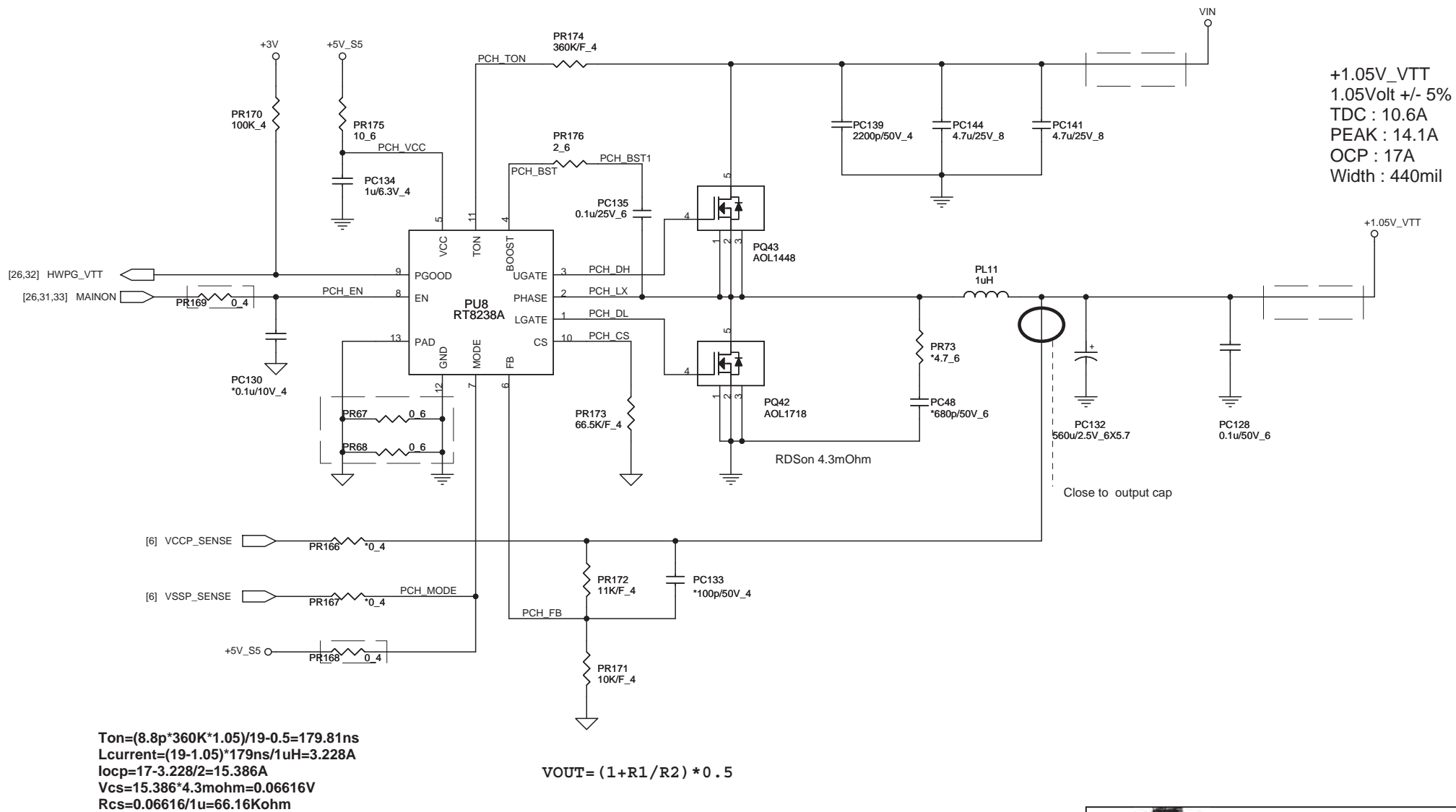
TDC : 2.25A  
PEAK : 3A  
Width : 100mil

TDC : 1.88A  
PEAK : 2.5A  
Width : 80mil

TDC : 2.74A  
PEAK : 3.65A  
Width : 110mil

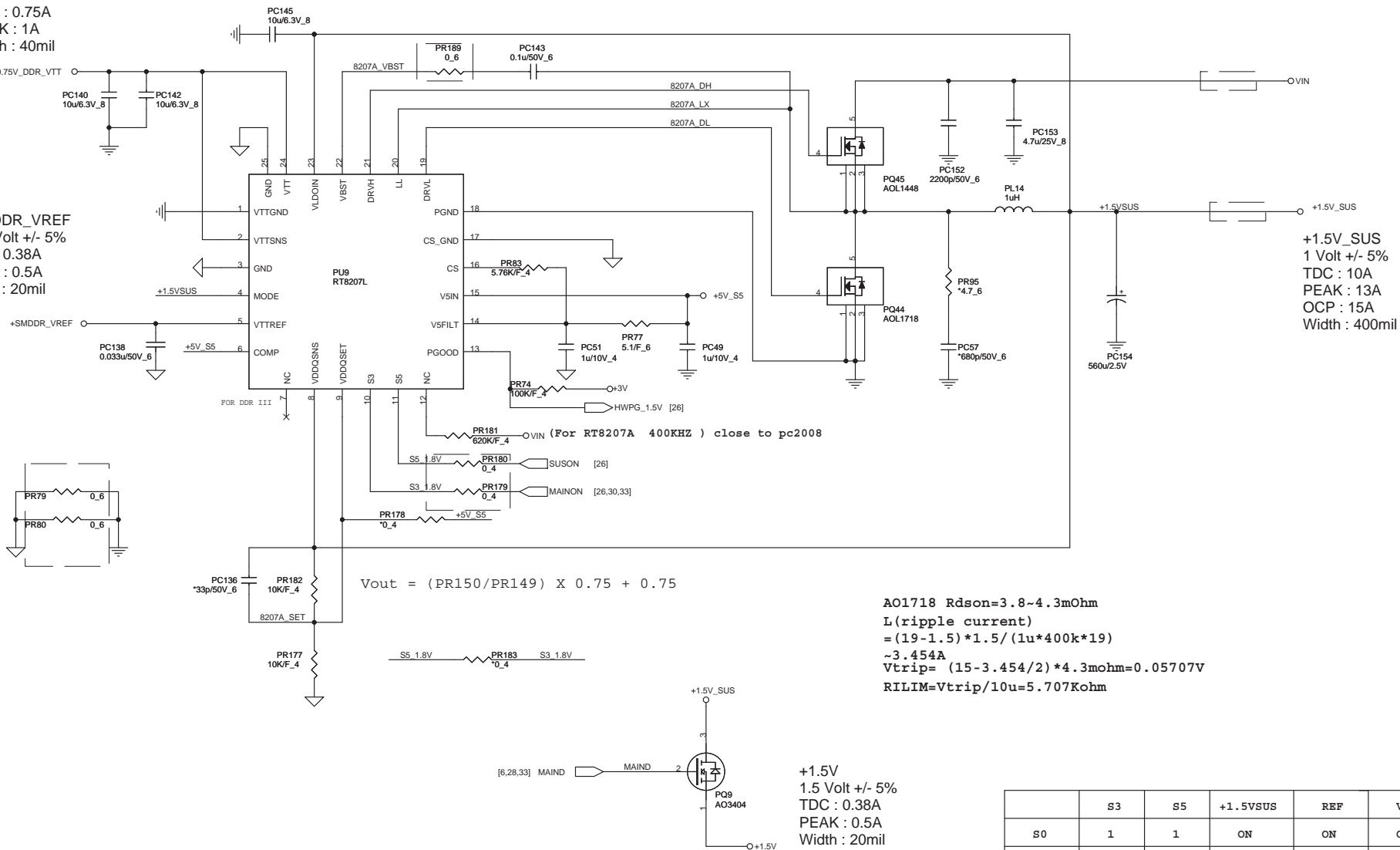
TDC : 0.16A  
PEAK : 0.21A  
Width : 10mil





+0.75V\_DDR\_VTT  
0.75 Volt +/- 5%  
TDC : 0.75A  
PEAK : 1A  
Width : 40mil

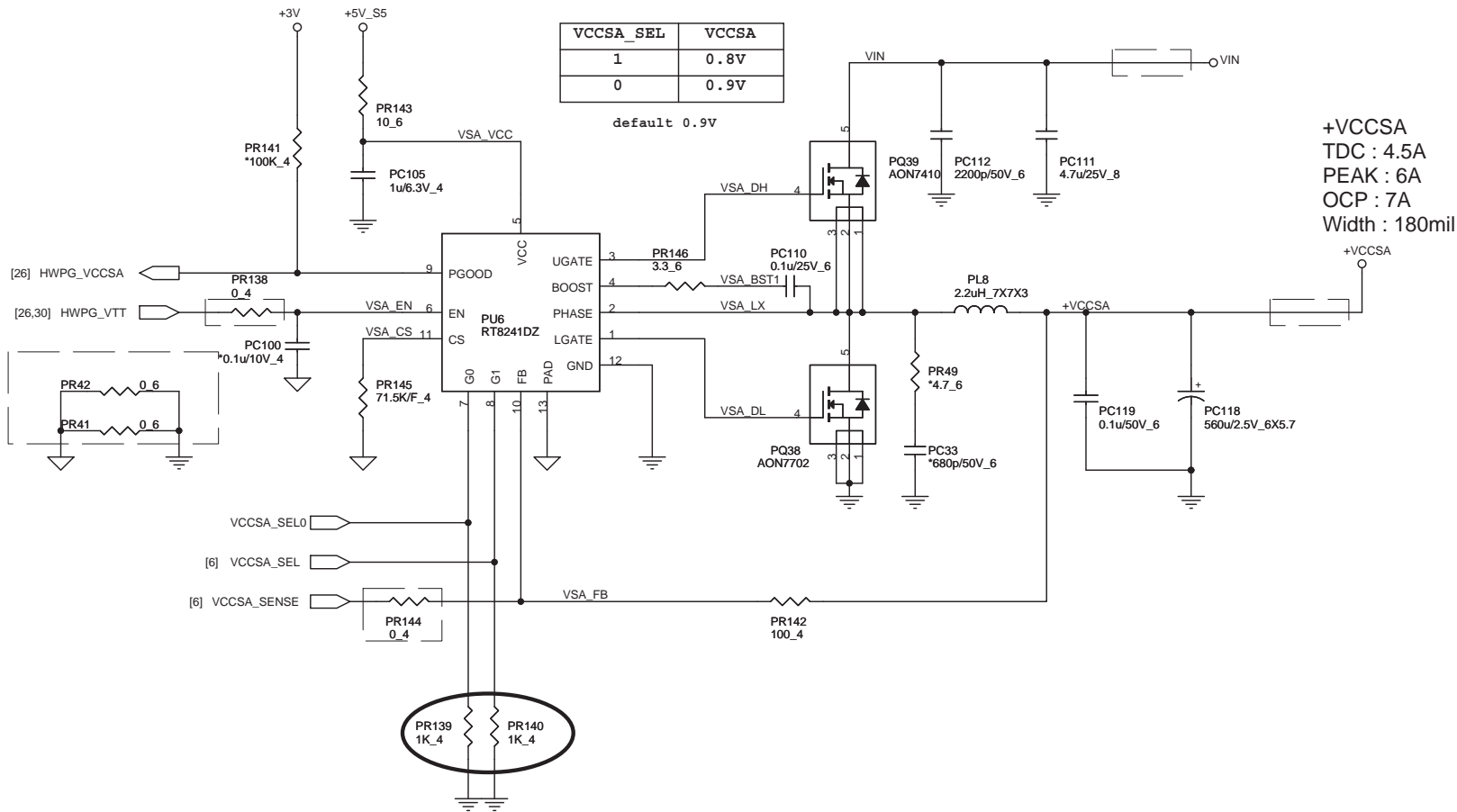
+SMDDR\_VREF  
0.75 Volt +/- 5%  
TDC : 0.38A  
PEAK : 0.5A  
Width : 20mil



G0	G1	VCCSA
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

VCCSA_SEL	VCCSA
1	0.8V
0	0.9V

default 0.9V



OCP=7A  
 $I_{ripple} = (19 - 0.9) \times 0.9 / (2.2 \times 300K \times 19)$   
 $= 1.299A$   
 $R_{th} = 14m\Omega \times 8 \times (7 - 0.65) / 10uA$   
 $= 71.125K$   
 $I_{peak} = 8.299A$



**Quanta Computer Inc.**  
**PROJECT : ZRL**

Size	Document Number	Rev
	<b>+VCCSA</b>	1A
Date:	Tuesday, June 21, 2011	Sheet 32 of 34





Model	date	CHANGE LIST	MODEL	ZRL
ZRL	5/18	page16 : L6,L8,L10 change to 0ohm C104,C86,C68 remove for monitor issue L5,L7,L9 change to 0603 package  page 8 : add R422 for GFX_PWRGD page 27 :PQ26,PQ28 change footprint page 17 :Remove U6 HDMI level shift page 9 :add Q26,R423 to separate CODEC SYNC signal page 22 :change R239,R240 to 47 ohm by realtek  5/25 page 29 : change PR133 to 1.58K, PR124 to 2.49K ,PC22,PC14 to 0.1u page 22 : remove Q25,Q24, stuff R236,R235 fix POPO sound  6/9 page 24 : change R246 to 33ohm,R245 to 68ohm, R247 to 150ohm for LED brightness.	FROM	To
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